

COMPAL CONFIDENTIAL

MODEL NAME : EDC42

PCB NO : LA-H171P

BOM P/N :

GPIO MAP: X10_WHL_KBL_CFLH_GPIO map Rev1.5_20180921

PWR Circuit: 14UMA_A00_PWR_20190308A

Brook Hollow 14 UMA (TBT)

Coffee Lake H

2019-03-20

REV : 1.0 (A00)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

5105@ : EC MEC5105 IC

5106@ : EC MEC5106 IC

WWAN@ : WWAN Component

WWANRF@ : WWAN RF Component

eSPI@ : eSPI interface

LPC@ : LPC interface

DS3@ : Deep sleep support

NDS3@ : non Deep sleep support

RTD3@ : RTD3 support

NRTD3@ : non RTD3 support

VPRO@ : VPRO support

NVPRO@ : non VPRO support

ST33@ : ST33 TPM support

750@ : NPCT750 TPM support

JUMP@ : Jump solder and short

@JUMP@ : Jump no solder

SATAPERI@ : Pericom SATA repeater support

SATAPARA@ : Parade SATA repeater support

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Cover Sheet

Size A Document Number LA-H171P Rev 0.1
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MB PCB

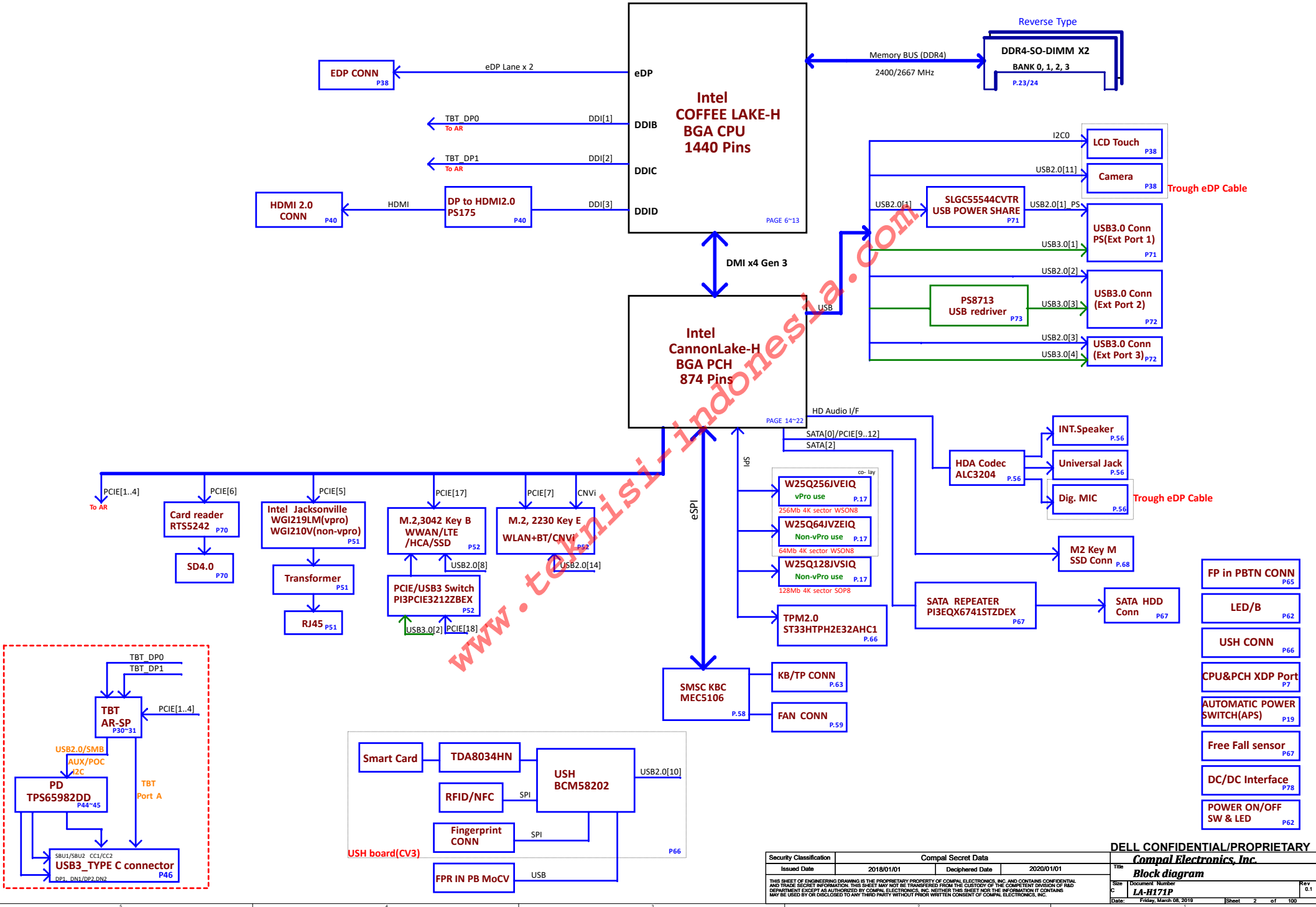
Part Number	Description
DAA000J2000	PCB 2FB LA-H171P REV0 MB 1

Layout Dell logo



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REV: A00
PWB: J11RG

Brook Hollow 14 UMA TBT Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
3	Sig 1		Copper foil	1oz	1.35
		3.6	Prepreg	2116HRCx2	8.90
4	GND1/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	4.00
5	Sig2		Copper foil	1oz	1.35
		3.6	Prepreg	2116HRCx2	8.20
6	Sig3		Copper foil	1oz	1.35
		3.6	Core	4mil	4.00
7	GND2		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)				47.2	46.60000 1.18364

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe #4	PCIe #5	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	SATA 0a	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	PCIe #18	PCIe #19	PCIe #20	PCIe #21	PCIe #22	PCIe #23	PCIe #24
Intel® RST Support								No Support	No Support						Yes		No Support			Yes				Yes		Yes				

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->RIGHT
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		Alpine Ridge - SP
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10	SATA-0A	
		PCIE-11	SATA-1A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 ->LEFT
3	JUSB3-->RIGHT
4	FP IN PB
5	TI PD
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	NA
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO
-----	---	-----

VIDEO	DESTINATION
eDP	LCD
DDI-B	Alpine Ridge - SP (Port 0)
DDI-C	Alpine Ridge - SP (Port 1)
DDI-D	PS175 --> JHDMI1

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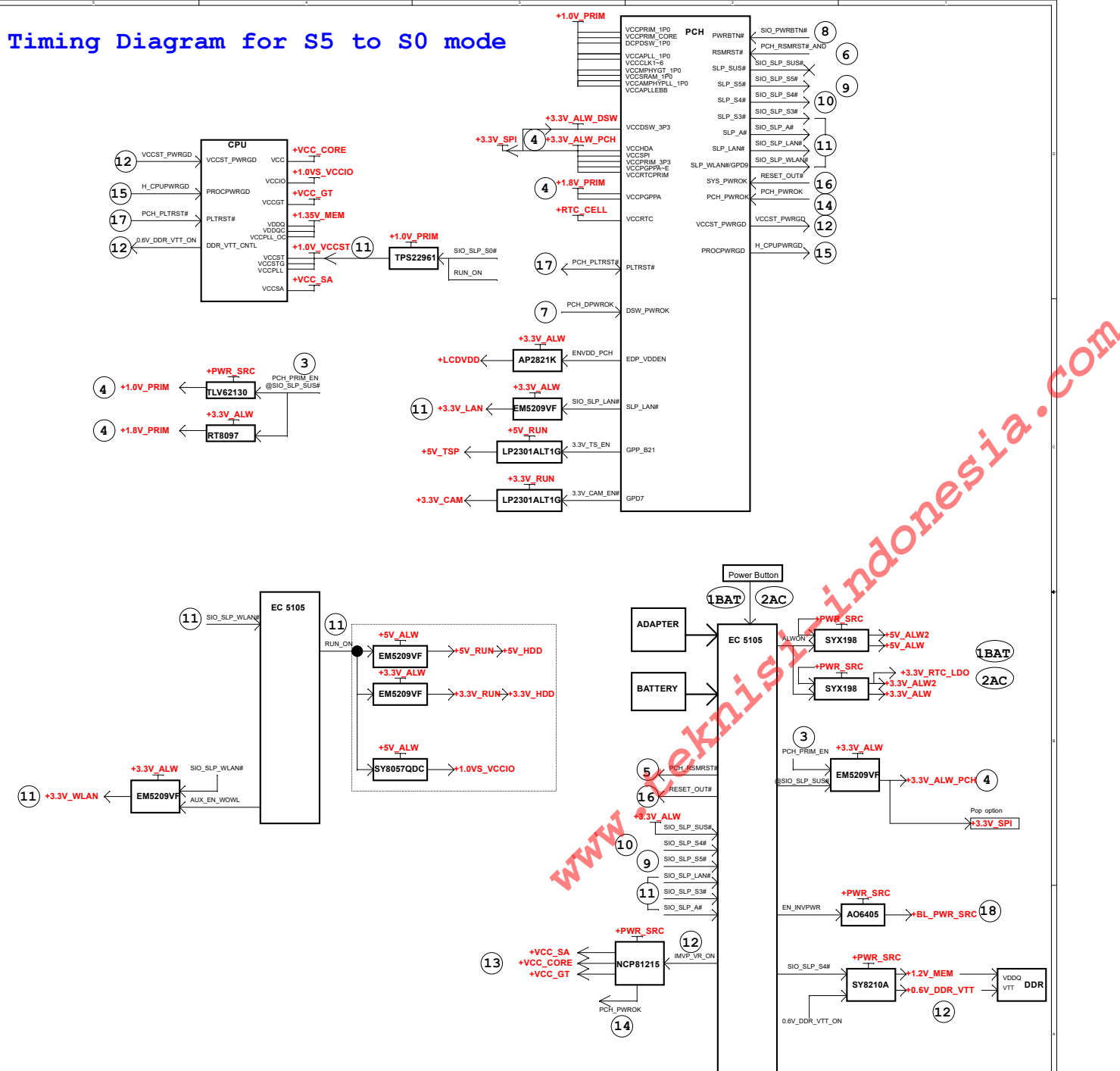
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Port Assignment

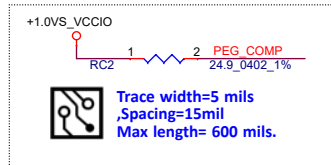
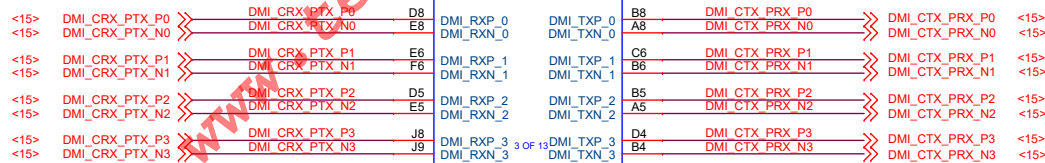
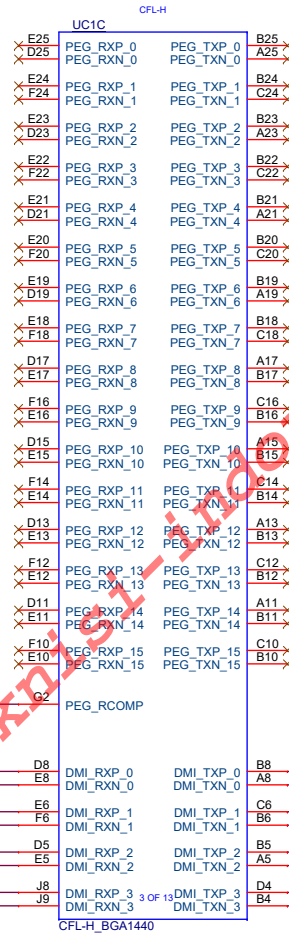
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Timing Diagram for S5 to S0 mode



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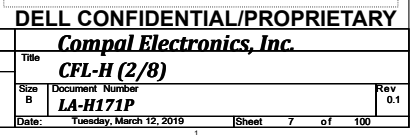
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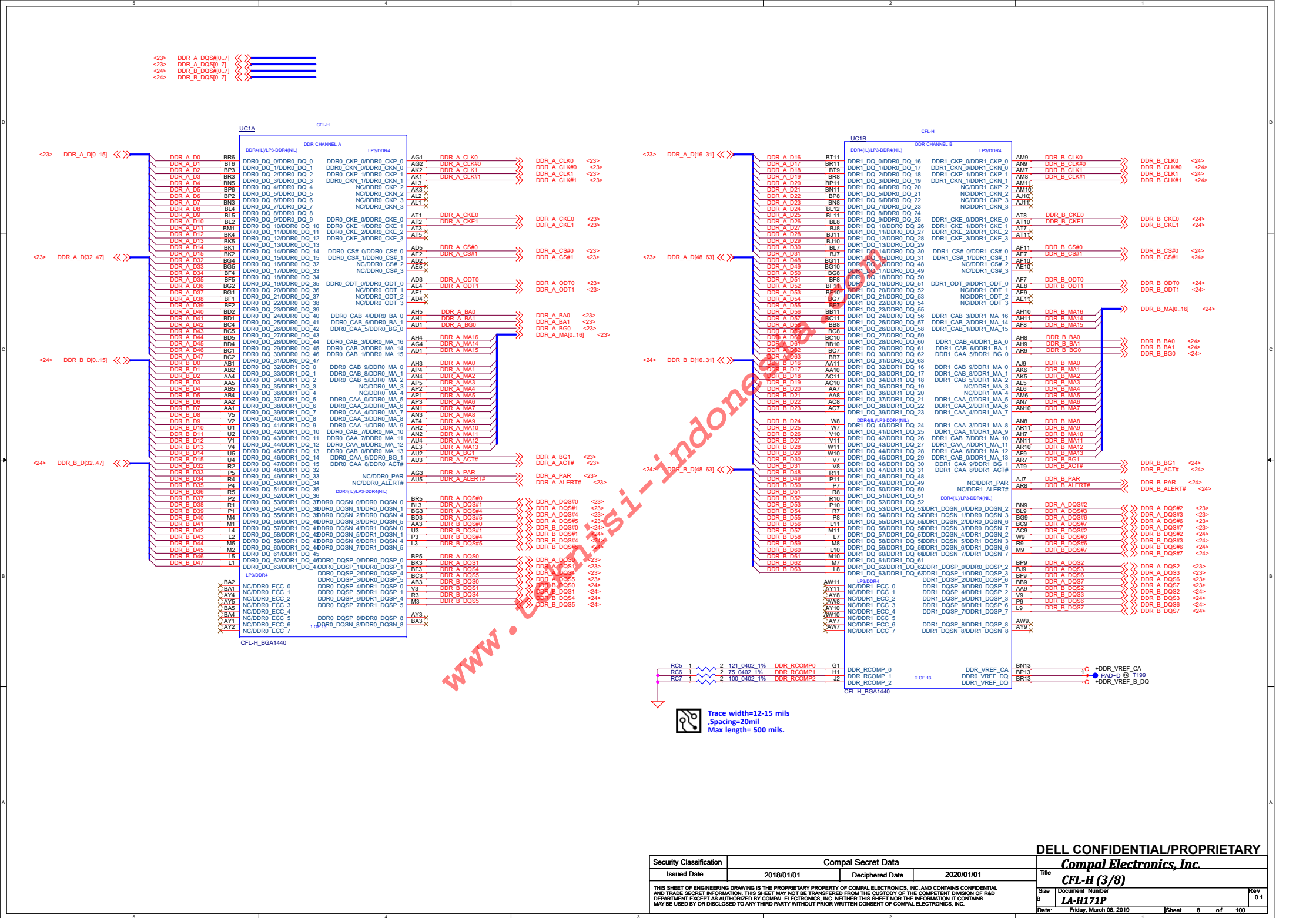
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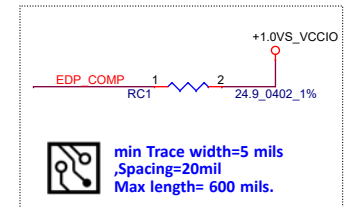
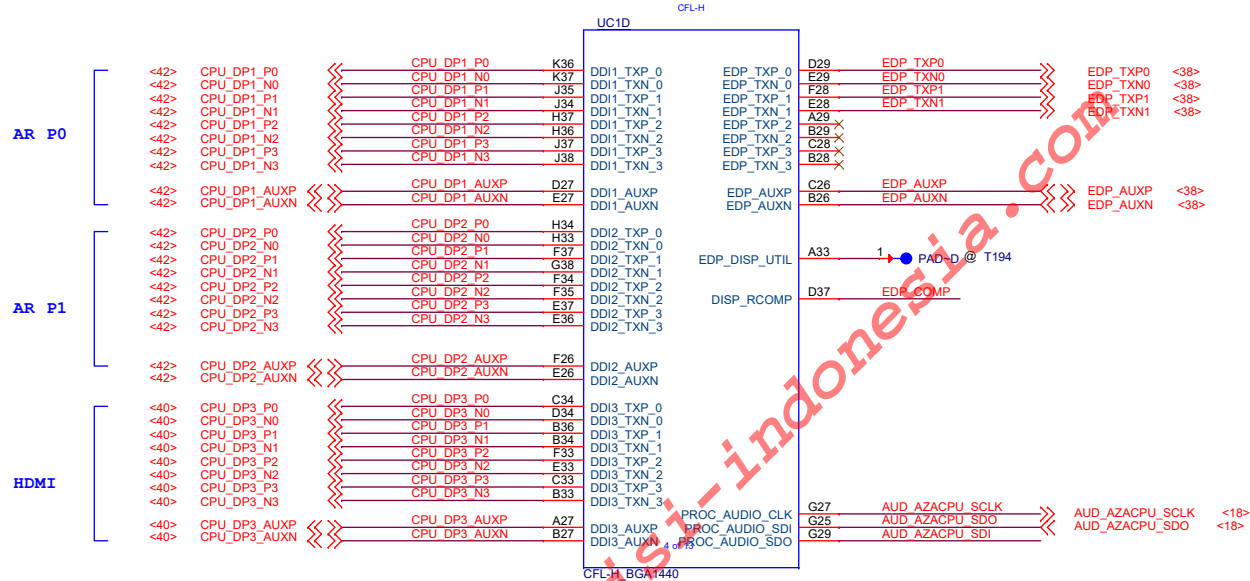
PEG Training

(default) PEG Train
immediately following

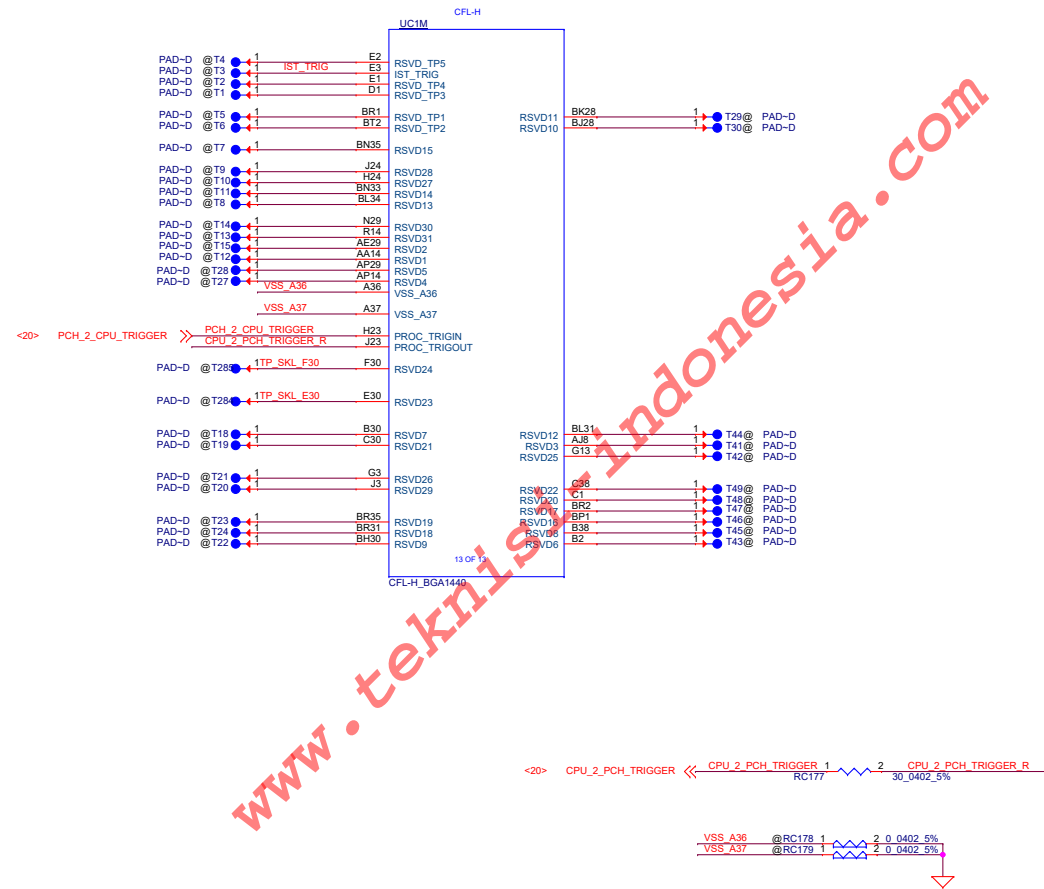
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										Size	
										Document Number	
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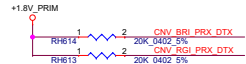
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A10	VSS 1	VSS 82				AL10		
A12	VSS 2	VSS 83				AL12		
A16	VSS 3	VSS 84				AL14		
A18	VSS 4	VSS 85				AL33		
A20	VSS 5	VSS 86				AL34		
A22	VSS 6	VSS 87				AL4		
A24	VSS 7	VSS 88				AL7		
A26	VSS 8	VSS 89				AL8		
A28	VSS 9	VSS 90				AL9		
A30	VSS 10	VSS 91				AM1		
A6	VSS 11	VSS 92				AM12		
A9	VSS 12	VSS 93				AM2		
AA12	VSS 13	VSS 94				AM3		
AA29	VSS 14	VSS 95				AM37		
AA30	VSS 15	VSS 96				AM38		
AB33	VSS 16	VSS 97				AM4		
AB34	VSS 17	VSS 98				AM5		
AB6	VSS 18	VSS 99				AN12		
AC1	VSS 19	VSS 100				AN29		
AC12	VSS 20	VSS 101				AN30		
AC2	VSS 21	VSS 102				AN6		
AC3	VSS 22	VSS 103				AP10		
AC37	VSS 23	VSS 104				AP11		
AC38	VSS 24	VSS 105				AP12		
AC4	VSS 25	VSS 106				AP3		
AC5	VSS 26	VSS 107				AP34		
AC6	VSS 27	VSS 108				AP8		
AD10	VSS 28	VSS 109				AP9		
AD11	VSS 29	VSS 110				AR1		
AD12	VSS 30	VSS 111				AR13		
AD29	VSS 31	VSS 112				AR14		
AD30	VSS 32	VSS 113				AR2		
AD6	VSS 33	VSS 114				AR29		
AD8	VSS 34	VSS 115				AR3		
AD9	VSS 35	VSS 116				AR30		
AE33	VSS 36	VSS 117				AR31		
AE34	VSS 37	VSS 118				AR32		
AE6	VSS 38	VSS 119				AR33		
AF1	VSS 39	VSS 120				AR34		
AF12	VSS 40	VSS 121				AR35		
AF13	VSS 41	VSS 122				AR36		
AF14	VSS 42	VSS 123				AR37		
AF2	VSS 43	VSS 124				AR38		
AF3	VSS 44	VSS 125				AR4		
AF4	VSS 45	VSS 126				AR5		
AG10	VSS 46	VSS 127				AT29		
AG11	VSS 47	VSS 128				AT30		
AG13	VSS 48	VSS 129				AT6		
AG29	VSS 49	VSS 130				AU10		
AG30	VSS 50	VSS 131				AU11		
AG6	VSS 51	VSS 132				AU12		
AG7	VSS 52	VSS 133				AU33		
AG8	VSS 53	VSS 134				AU34		
AH12	VSS 54	VSS 135				AU6		
AH33	VSS 55	VSS 136				AU7		
AH34	VSS 56	VSS 137				AU8		
AH35	VSS 57	VSS 138				AU9		
AH36	VSS 58	VSS 139				AV37		
AH6	VSS 59	VSS 140				AV38		
AJ1	VSS 60	VSS 141				AW1		
AJ13	VSS 61	VSS 142				AW12		
AJ2	VSS 62	VSS 143				AW2		
AJ3	VSS 63	VSS 144				AW29		
AJ37	VSS 64	VSS 145				AW3		
AJ38	VSS 65	VSS 146				AW30		
AJ4	VSS 66	VSS 147				AW4		
AJ5	VSS 67	VSS 148				U6		
AJ6	VSS 68	VSS 149				V29		
W4	VSS 69	VSS 150				V30		
W5	VSS 70	VSS 151				A14		
Y10	VSS 71	VSS 152				AD7		
Y11	VSS 72	VSS 153				V6		
Y13	VSS 73	VSS 154				W1		
Y14	VSS 74	VSS 155				W12		
Y37	VSS 75	VSS 156				W2		
Y38	VSS 76	VSS 157				W3		
Y7	VSS 77	VSS 158				W33		
Y8	VSS 78	VSS 159				W34		
Y9	VSS 79	VSS 160						
AK29	VSS 80	VSS 161						
AK30	VSS 81	VSS 162						

CFL-H_BGA1440

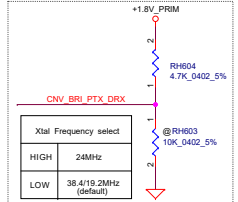
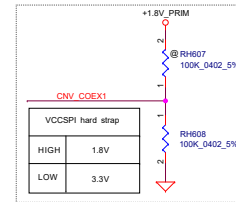
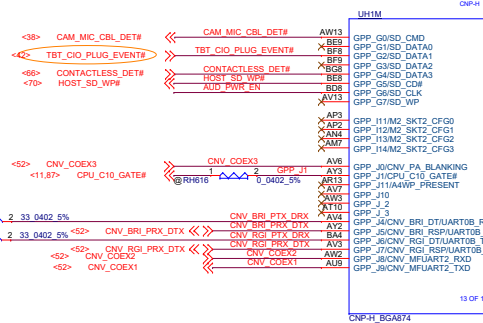
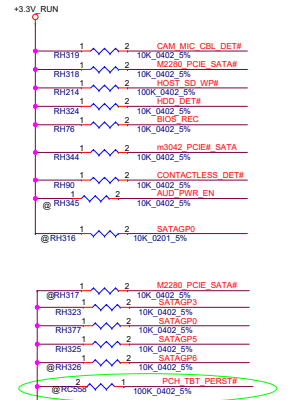
CFL-H			UC1G			BJ15		
AW5	VSS 163	VSS 244				BJ18		
AY12	VSS 164	VSS 245				BJ22		
AY33	VSS 165	VSS 246				BJ25		
AY34	VSS 166	VSS 247				BJ29		
B9	VSS 167	VSS 248				BJ30		
BA10	VSS 168	VSS 249				BJ31		
BA11	VSS 169	VSS 250				BJ32		
BA12	VSS 170	VSS 251				BJ33		
BA37	VSS 171	VSS 252				BJ34		
BA38	VSS 172	VSS 253				BJ35		
BA6	VSS 173	VSS 254				BJ36		
BA7	VSS 174	VSS 255				BK13		
BA8	VSS 175	VSS 256				BK14		
BA9	VSS 176	VSS 257				BK15		
BB1	VSS 177	VSS 258				BK18		
BB12	VSS 178	VSS 259				BK22		
BB2	VSS 179	VSS 260				BK25		
BB29	VSS 180	VSS 261				BK29		
BB3	VSS 181	VSS 262				BK6		
BB30	VSS 182	VSS 263				BL13		
BB4	VSS 183	VSS 264				BL14		
BB5	VSS 184	VSS 265				BL18		
BB6	VSS 185	VSS 266				BL19		
BC12	VSS 186	VSS 267				BL20		
BC13	VSS 187	VSS 268				BL21		
BC14	VSS 188	VSS 269				BL22		
BC33	VSS 189	VSS 270				BL29		
BC34	VSS 190	VSS 271				BL33		
BC6	VSS 191	VSS 272				BL35		
BD010	VSS 192	VSS 273				BL38		
BD11	VSS 193	VSS 274				BL6		
BD12	VSS 194	VSS 275				BM11		
BD37	VSS 195	VSS 276				BM12		
BD6	VSS 196	VSS 277				BM13		
BD7	VSS 197	VSS 278				BM14		
BD8	VSS 198	VSS 279				BM17		
BD9	VSS 199	VSS 280				BM2		
BE1	VSS 200	VSS 281				BM21		
BE2	VSS 201	VSS 282				BM22		
BE29	VSS 202	VSS 283				BM23		
BE3	VSS 203	VSS 284				BM24		
BE30	VSS 204	VSS 285				BM25		
BE4	VSS 205	VSS 286				BM26		
BE5	VSS 206	VSS 287				BM27		
BE6	VSS 207	VSS 288				BM28		
BF12	VSS 208	VSS 289				BM29		
BF33	VSS 209	VSS 290				BM3		
BF34	VSS 210	VSS 291				BM33		
BF6	VSS 211	VSS 292				BM35		
BG12	VSS 212	VSS 293				BM38		
BG13	VSS 213	VSS 294				BM5		
BG14	VSS 214	VSS 295				BM6		
BG37	VSS 215	VSS 296				BM7		
BG38	VSS 216	VSS 297				BM8		
BG6	VSS 217	VSS 298				BM9		
BH1	VSS 218	VSS 299				BN12		
BH10	VSS 219	VSS 300				BN14		
BH11	VSS 220	VSS 301				BN18		
BH12	VSS 221	VSS 302				BN19		
BH14	VSS 222	VSS 303				BN2		
BH2	VSS 223	VSS 304				BN20		
BH3	VSS 224	VSS 305				BN21		
BH4	VSS 225	VSS 306				BN24		
BH5	VSS 226	VSS 307				BN29		
BH6	VSS 227	VSS 308				BN30		
BH7	VSS 228	VSS 309				BN31		
BH8	VSS 229	VSS 310				BN34		
BH9	VSS 230	VSS 311				P38		
T2	VSS 231	VSS 312				P6		
T3	VSS 232	VSS 313				R12		
T33	VSS 233	VSS 314				R29		
T34	VSS 234	VSS 315				AY14		
T4	VSS 235	VSS 316				R30		
T5	VSS 236	VSS 317				T1		
T7	VSS 237	VSS 318				T10		
W1	VSS 238	VSS 319				T11		
T8	VSS 239	VSS 320				T12		
T9	VSS 240	VSS 321				T13		
U37	VSS 241	VSS 322				T14		
U38	VSS 242	VSS 323						
U39	VSS 243	VSS 324						
BJ12								
BJ14								

CFL-H_BGA1440

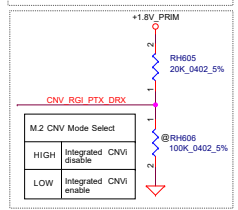
CFL-H			UC1H					
BN4	VSS 325	VSS 409				F15		
BN7	VSS 326	VSS 410				F17		
BP12	VSS 327	VSS 411				F19		
BP14	VSS 328	VSS 412				F2		
BP18	VSS 329	VSS 413				F21		
BP21	VSS 329	VSS 413				F23		
BP24	VSS 330	VSS 414				F25		
BP25	VSS 331	VSS 415				F27		
BP26	VSS 332	VSS 416				F29		
BP29	VSS 334	VSS 418				F3		
BP33	VSS 335	VSS 419				F31		
BP34	VSS 335	VSS 419				F36		
BP7	VSS 336	VSS 420				F4		
BR12	VSS 337	VSS 421				F5		
BR14	VSS 338	VSS 422				F8		
BR18	VSS 340	VSS 424				F9		
BR21	VSS 341	VSS 425				G10		
BR24	VSS 342	VSS 426				G12		
BR25	VSS 342	VSS 426				G14		
BR26	VSS 343	VSS 427				G16		
BR29	VSS 344	VSS 428				G18		
BR34	VSS 345	VSS 429				G20		
BR36	VSS 346	VSS 430				G22		
BR7	VSS 347	VSS 431				G23		
BT12	VSS 348	VSS 432				G24		
BT14	VSS 349	VSS 433				G26		
BT18	VSS 350	VSS 434				G28		
BT21	VSS 351	VSS 435				G4		
BT24	VSS 352	VSS 436				G5		
BT26	VSS 353	VSS 437				G6		
BT29	VSS 354	VSS 438				G8		
BT32	VSS 355	VSS 439				G9		
BT5	VSS 356	VSS 440				H11		
C11	VSS 357	VSS 441				H12		
C13	VSS 358	VSS 442				H18		
C15	VSS 359	VSS 443				H25		
C17	VSS 360	VSS 444				H32		
C19	VSS 361	VSS 445				H40		
C21	VSS 362	VSS 446				H35		
C23	VSS 363	VSS 447				J10		
C25	VSS 364	VSS 448				J18		
C27	VSS 365	VSS 449				J25		
C29	VSS 366	VSS 450				J2		
C31	VSS 367	VSS 451				J5		
C37	VSS 368	VSS 452				J33		
C5	VSS 369	VSS 453				J36		
C8	VSS 370	VSS 454				J4		
C9	VSS 371	VSS 455				K1		
D10	VSS 372	VSS 456				K10		
D12	VSS 373	VSS 457				K11		
D14	VSS 374	VSS 458				K2		
D16	VSS 375	VSS 459				K2		
D18	VSS 376	VSS 460				K3		
D20	VSS 377	VSS 461				K38		
D22	VSS 378	VSS 462				K4		
D24	VSS 379	VSS 463				K4		
D26	VSS 380	VSS 464				K7		
D28	VSS 381	VSS 465				K8		
D3	VSS 382	VSS 466				K9		
D30	VSS 383	VSS 467				L29		
D33	VSS 384	VSS 468				L30		
D6	VSS 385	VSS 469				L33		
D9	VSS 386	VSS 470				L34		
E34	VSS 387	VSS 471				M12		
E35	VSS 388	VSS 472				M13		
E38	VSS 389	VSS 473				N10		
E4	VSS 390	VSS 474				N11		
E9	VSS 391	VSS 475				N12		
N3	VSS 392	VSS 476				N2		
N33	VSS 393	VSS 477				B18		
N34	VSS 394	VSS 478				BR9		
N4	VSS 395	VSS 479						
N5	VSS 396							
N6	VSS 397	VSS A3				A3		
N7	VSS 398	VSS A34				A34		
N8	VSS 399	VSS A4				A3		
N9	VSS 400	VSS B3				B37		
P12	VSS 401	VSS B37				BR38		
P37	VSS 402	VSS BR38				BT3		
M14	VSS 403	VSS BT3				BT35		
M6	VSS 404	VSS BT34				BT36		
N1	VSS 405	VSS BT36				B14		
F11	VSS 406	VSS BT4				C2		
F13	VSS 407	VSS C2				C38		
	VSS 408	VSS D38						



CFL PDG rev0.5
To avoid floating input at the I/O pin it is recommended to add a weak pull-up resistor to the SOC pin with a recommended value of 20K ohm.

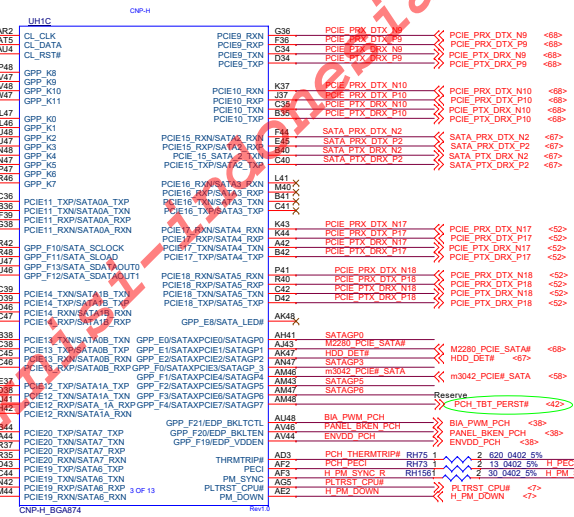


CNP EDS rev0.7
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.



M.2 Socket 3 (Key M)

M.2 Socket 3 (Key M)



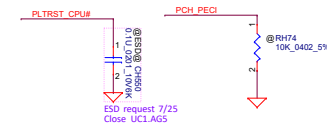
M.2 Socket 3 (Key M)

SATA HDD

M.2 3042 HCA or QCA LTE SSD Cache

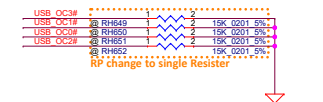
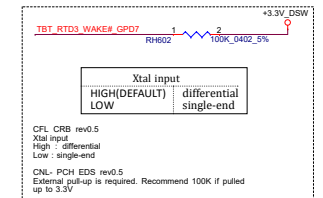
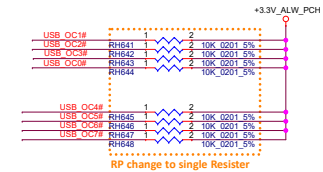
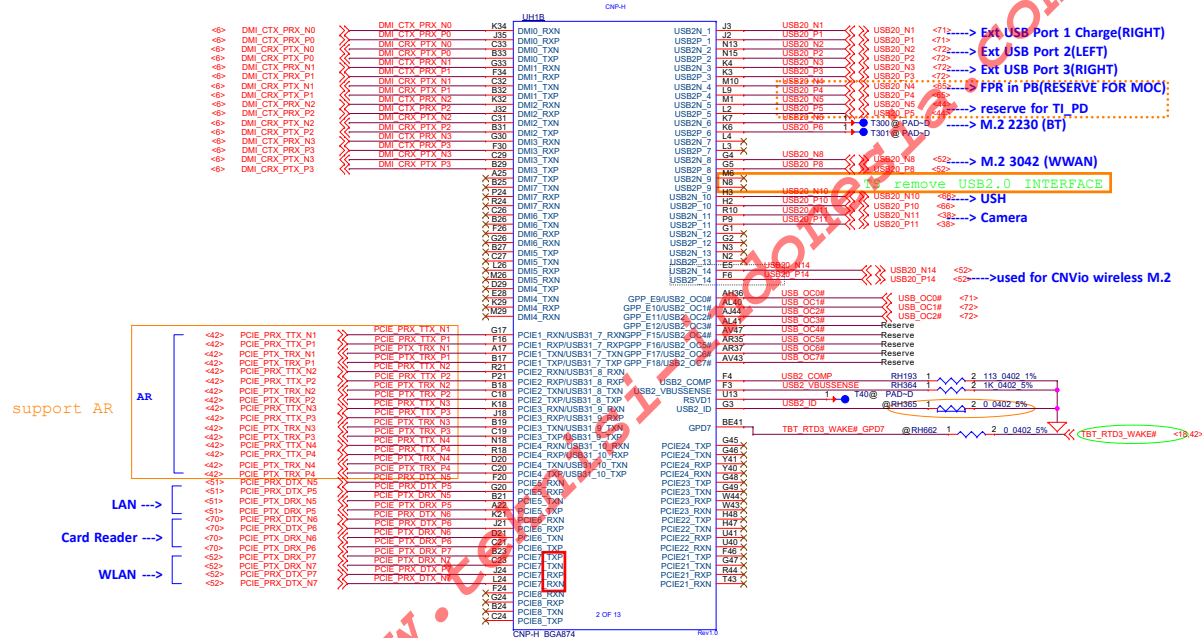
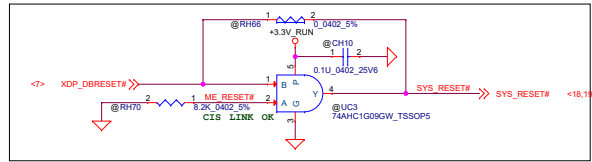
M.2 3042 HCA or QCA LTE SSD Cache

SPSGP0	0	SATAGP0	1=SATA	0=PCIE
SPSGP1	1	m2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	n3042_PCIE#_SATA	1=SATA	0=PCIE
SPSGP5	0	SPTAGP5	1=SATA	0=PCIE

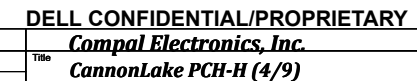


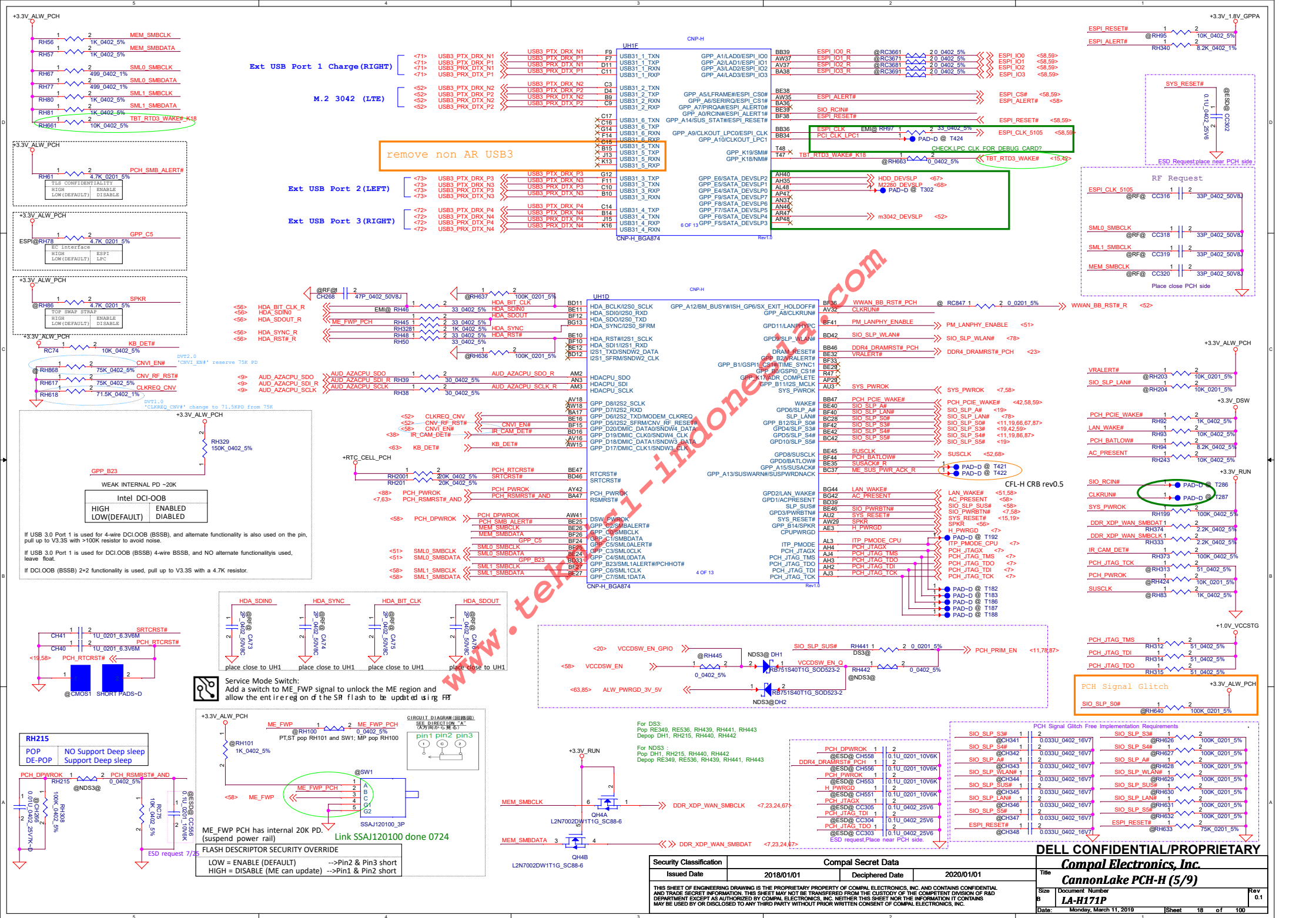
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Compal Electronics, Inc.
CannonLake PCH-H (1/9)

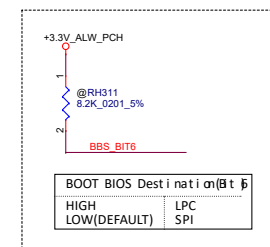
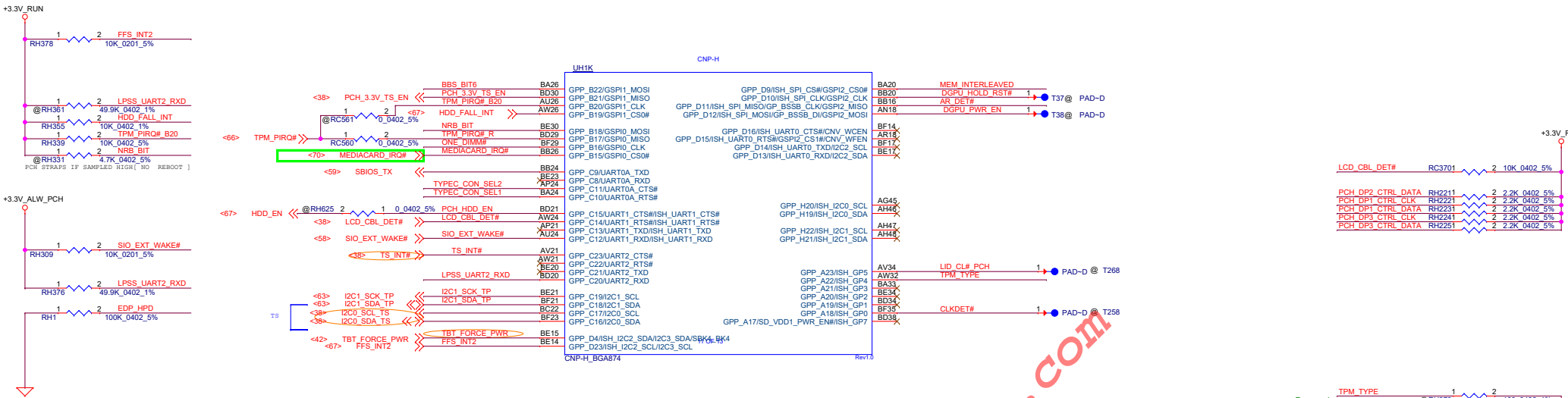
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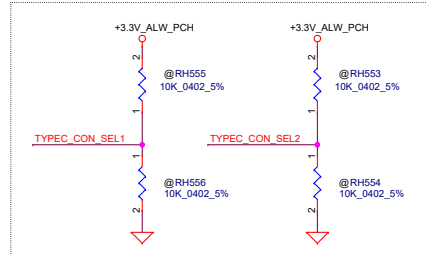
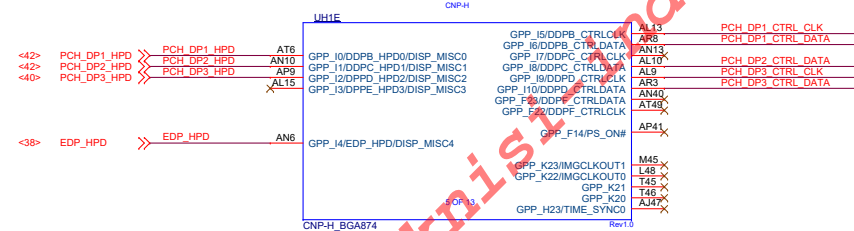
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Issued Date				2018/01/01				Compal Electronics, Inc.			
Deciphered Date				2020/01/01				CannonLake PCH-H (2/9)			
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Date				Monday, March 11, 2019				15 of 100			



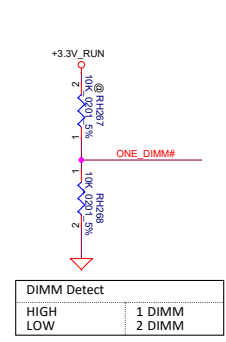




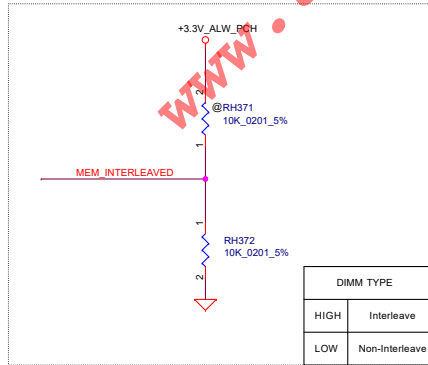
BOOT BIOS Destination (Bit 6)	
HIGH	LPC
LOW (DEFAULT)	SPI



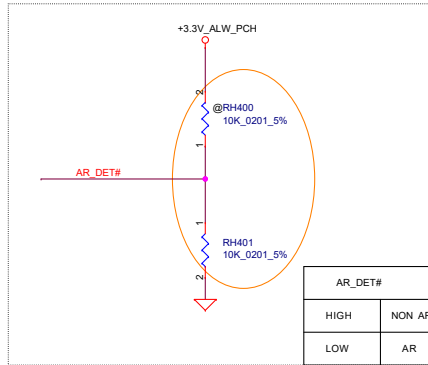
Vendor	JAE	FOXCON	TBD	TBD
TYPECON_SEL1	LOW	LOW	HIGH	HIGH
TYPECON_SEL2	LOW	HIGH	LOW	HIGH



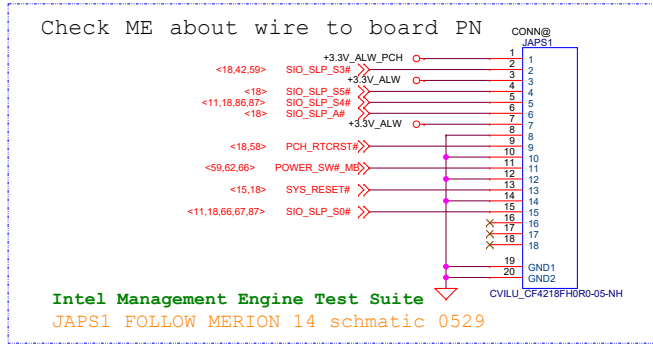
DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM



DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave



AR_DET#	
HIGH	NON AR
LOW	AR



Intel Management Engine Test Suite
JAPS1 FOLLOW MERION 14 schmatic 0529

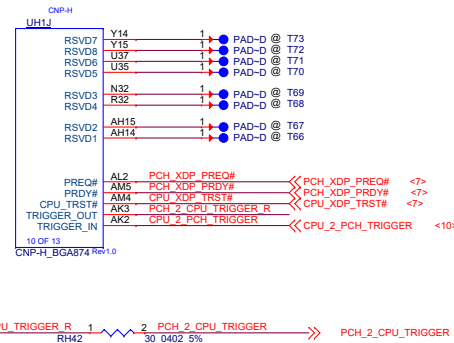
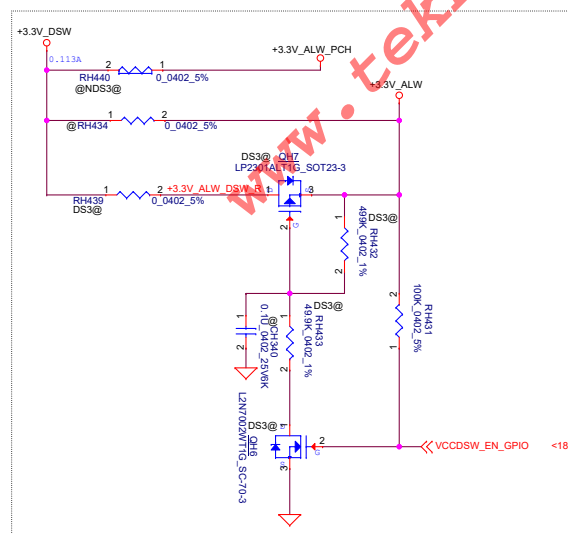
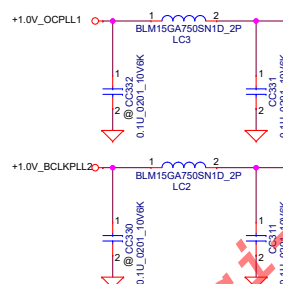
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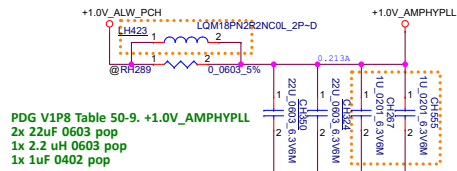
CanonLake PCH-H (6/9)

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Title	CanonLake PCH-H (6/9)	
Size	Document Number	Rev
B	LA-H171P	0.1
Date:	Friday, March 08, 2019	Sheet 19 of 100

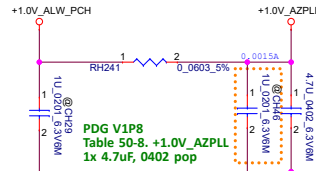


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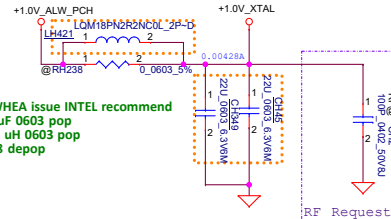
PDG V1P8 Table 50-9. +1.0V_AMPHYPLL
2x 22uF 0603 pop
1x 2.2 uH 0603 pop
1x 1uF 0402 pop

8/15 downsize to SE00000UC00 add 1 uF



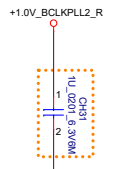
PDG V1P8
Table 50-8. +1.0V_AZPLL
1x 4.7uF, 0402 pop

8/15 downsize to SE00000UC00

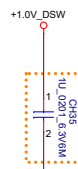


KBL WHEA issue INTEL recommend
2x 22uF 0603 pop
1x 2.2 uH 0603 pop
RH238 depop

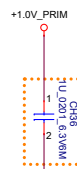
RF Request



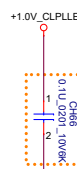
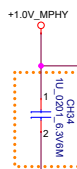
8/15 downsize to SE00000UC00



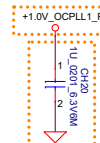
8/15 downsize to SE00000UC00



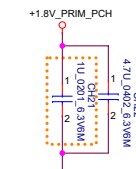
8/15 downsize to SE00000SV00



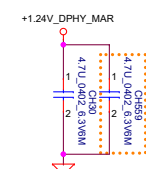
8/15 downsize to SE00000SV00



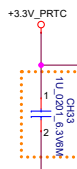
CH20 close PCH
8/15 downsize to SE00000UC00



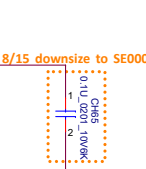
8/15 downsize to SE00000UC00



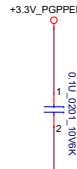
8/17 add one more 4.7 uF



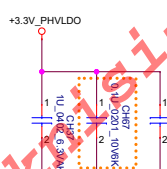
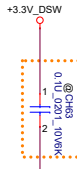
8/15 downsize to SE00000UC00



8/15 downsize to SE00000SV00



8/15 downsize to SE00000SV00



8/15 downsize to SE00000SV00

CFL-H PDG rev0.5
4.7uF x1

CRB-H rev0.7
0.1uF x1, 1uF x1

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CannonLake PCH-H (8/9)

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				Date:	Monday, March 11, 2019
				Sheet	21 of 100

CNP-H			
UH1L		AL12	
A2	VSS_1	VSS_73	AL17
A28	VSS_2	VSS_74	AL21
A3	VSS_3	VSS_75	AL24
A33	VSS_4	VSS_76	AL26
A37	VSS_5	VSS_77	AL28
A4	VSS_6	VSS_78	AL33
A45	VSS_7	VSS_79	AL38
A46	VSS_8	VSS_80	AM1
A47	VSS_9	VSS_81	AM18
A48	VSS_10	VSS_82	AM32
A5	VSS_11	VSS_83	AM40
A8	VSS_12	VSS_84	AN12
AA19	VSS_13	VSS_85	AN16
AA20	VSS_14	VSS_86	AN34
AA25	VSS_15	VSS_87	AN38
AA27	VSS_16	VSS_88	AP4
AA28	VSS_17	VSS_89	AP46
AA30	VSS_18	VSS_90	AR12
AA31	VSS_19	VSS_91	AR16
AA49	VSS_20	VSS_92	AR34
AA5	VSS_21	VSS_93	AR38
AB19	VSS_22	VSS_94	AT1
AB25	VSS_23	VSS_95	AT16
AB31	VSS_24	VSS_96	AT18
AC12	VSS_25	VSS_97	AT21
AC17	VSS_26	VSS_98	AT24
AC33	VSS_27	VSS_99	AT26
AC38	VSS_28	VSS_100	AT29
AC4	VSS_29	VSS_101	AT32
AC46	VSS_30	VSS_102	AT34
AD1	VSS_31	VSS_103	AT45
AD19	VSS_32	VSS_104	AV11
AD2	VSS_33	VSS_105	AV39
AD22	VSS_34	VSS_106	AW10
AD49	VSS_35	VSS_107	AW4
AE12	VSS_36	VSS_108	AW40
AE33	VSS_37	VSS_109	AW46
AE38	VSS_38	VSS_110	B47
AE4	VSS_39	VSS_111	B48
AE46	VSS_40	VSS_112	B49
AF22	VSS_41	VSS_113	BA12
AF25	VSS_42	VSS_114	BA14
AF28	VSS_43	VSS_115	BA44
AG1	VSS_44	VSS_116	BA5
AG22	VSS_45	VSS_117	BA6
AG23	VSS_46	VSS_118	BB41
AG25	VSS_47	VSS_119	BB43
AG27	VSS_48	VSS_120	BB9
AG28	VSS_49	VSS_121	BC10
AG30	VSS_50	VSS_122	BC15
AG49	VSS_51	VSS_123	BC15
AH12	VSS_52	VSS_124	BC19
AH17	VSS_53	VSS_125	BC24
AH33	VSS_54	VSS_126	BC28
AH38	VSS_55	VSS_127	BC31
AJ19	VSS_56	VSS_128	BC35
AJ20	VSS_57	VSS_129	BC40
AJ25	VSS_58	VSS_130	BC45
AJ27	VSS_59	VSS_131	BC6
AJ28	VSS_60	VSS_132	BD43
AJ30	VSS_61	VSS_133	BE44
AJ31	VSS_62	VSS_134	BF1
AK19	VSS_63	VSS_135	BF2
AK20	VSS_64	VSS_136	BF3
AK25	VSS_65	VSS_137	BF48
AK27	VSS_66	VSS_138	BF49
AK28	VSS_67	VSS_139	BG17
AK30	VSS_68	VSS_140	BG2
AK31	VSS_69	VSS_141	BG22
AK4	VSS_70	VSS_142	BG25
AK46	VSS_71	VSS_143	BG28
	VSS_72	VSS_144	

CNP-H_BGA874 Rev1.3

CNP-H			
UH1L		M24	
BG3	VSS_145	VSS_196	M32
BG33	VSS_146	VSS_197	M34
BG37	VSS_147	VSS_198	M49
BG4	VSS_148	VSS_199	M5
BG46	VSS_149	VSS_200	N12
C12	VSS_150	VSS_201	N16
C25	VSS_151	VSS_202	N34
C30	VSS_152	VSS_203	N35
C4	VSS_153	VSS_204	N37
C48	VSS_154	VSS_205	N38
C5	VSS_155	VSS_206	P26
D12	VSS_156	VSS_207	P28
D16	VSS_157	VSS_208	P49
D17	VSS_158	VSS_209	P46
D30	VSS_159	VSS_210	R12
D33	VSS_160	VSS_211	R16
D6	VSS_161	VSS_212	R26
E10	VSS_162	VSS_213	R29
E13	VSS_163	VSS_214	R3
E15	VSS_164	VSS_215	R34
E17	VSS_165	VSS_216	R38
E19	VSS_166	VSS_217	R4
E22	VSS_167	VSS_218	T17
E24	VSS_168	VSS_219	T18
E26	VSS_169	VSS_220	T4
E31	VSS_170	VSS_221	T32
E33	VSS_171	VSS_222	T49
E35	VSS_172	VSS_223	T5
E40	VSS_173	VSS_224	T7
E42	VSS_174	VSS_225	U12
E8	VSS_175	VSS_226	U15
F41	VSS_176	VSS_227	U17
F43	VSS_177	VSS_228	U21
F47	VSS_178	VSS_229	U24
G44	VSS_179	VSS_230	U33
G6	VSS_180	VSS_231	U38
H8	VSS_181	VSS_232	V20
J10	VSS_182	VSS_233	V22
J26	VSS_183	VSS_234	V4
J29	VSS_184	VSS_235	V46
J4	VSS_185	VSS_236	W25
J40	VSS_186	VSS_237	W27
J46	VSS_187	VSS_238	W28
J47	VSS_188	VSS_239	W30
J48	VSS_189	VSS_240	Y10
J9	VSS_190	VSS_241	Y12
K11	VSS_191	VSS_242	Y17
K39	VSS_192	VSS_243	Y33
M16	VSS_193	VSS_244	Y38
M18	VSS_194	VSS_245	Y9
M21	VSS_195	VSS_246	

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DGPU DC/DC Interface

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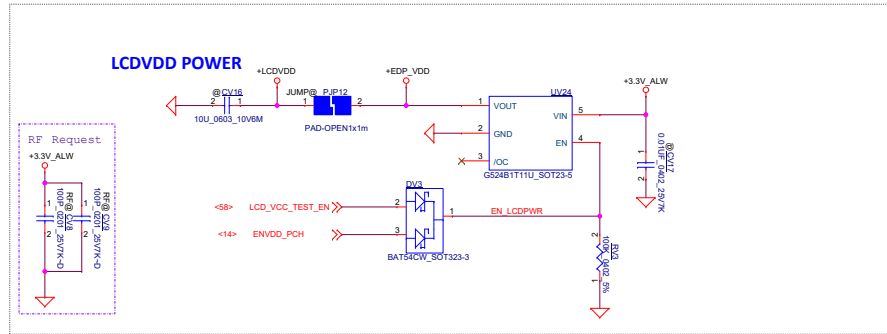
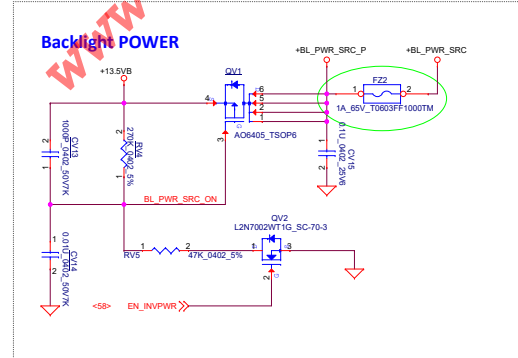
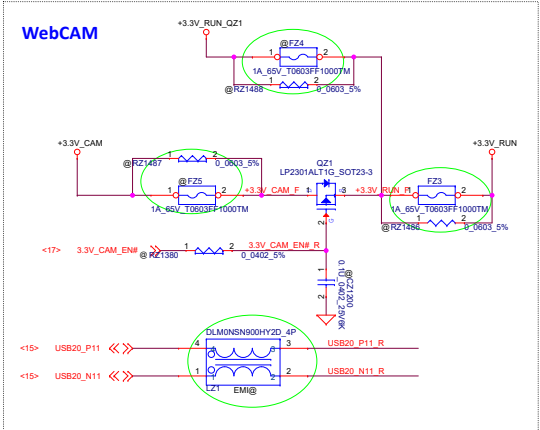
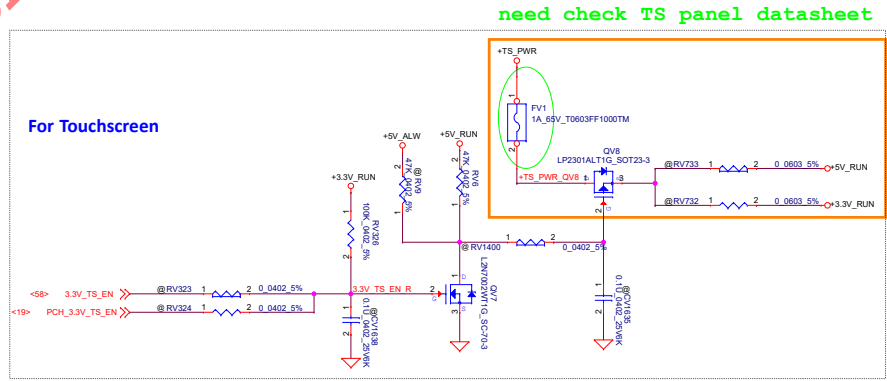
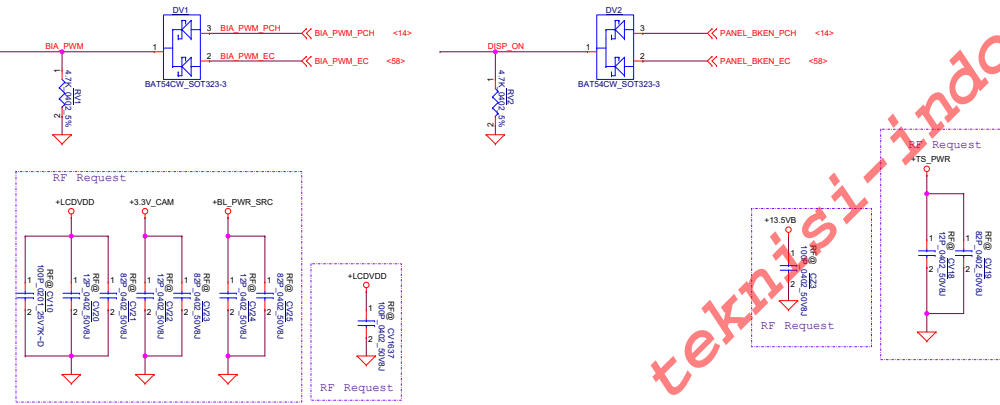
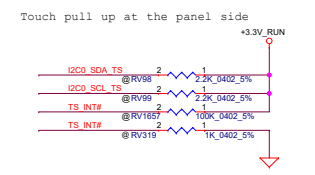
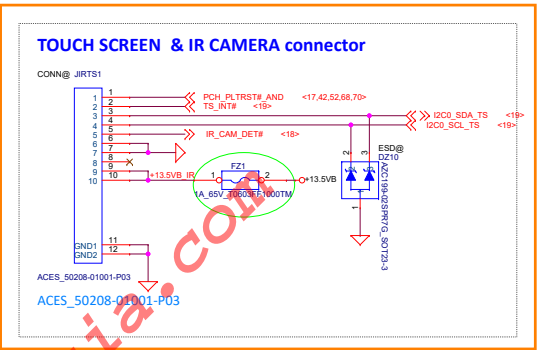
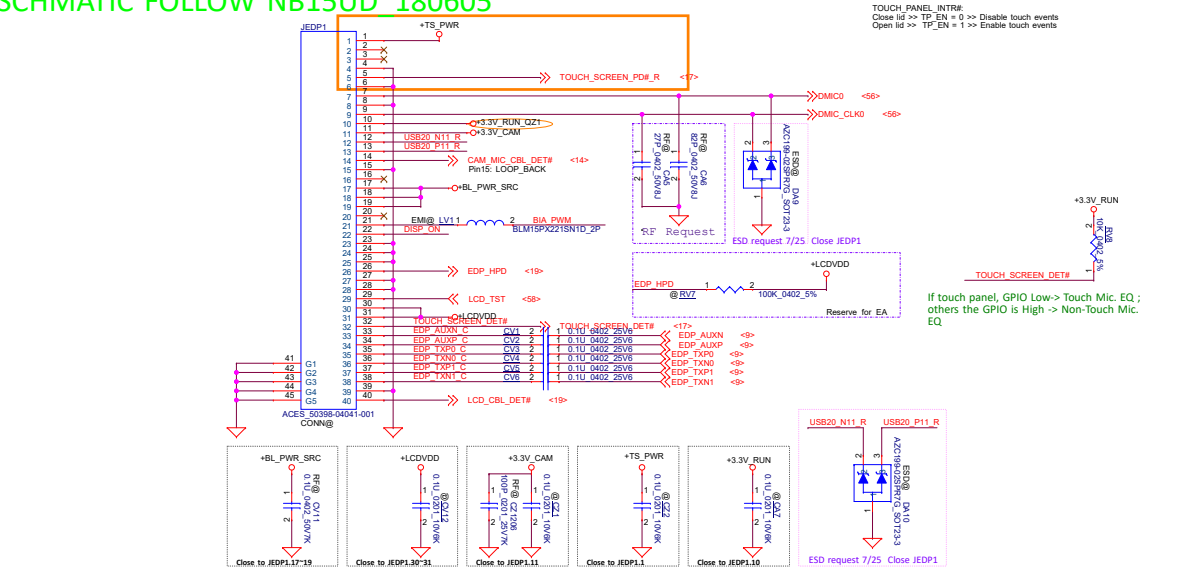
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Rev 0.1

BH JEDP1,JIRTS1 PINDEFINE FOLLOW NB
SCHMATIC FOLLOW NB15UD 180605



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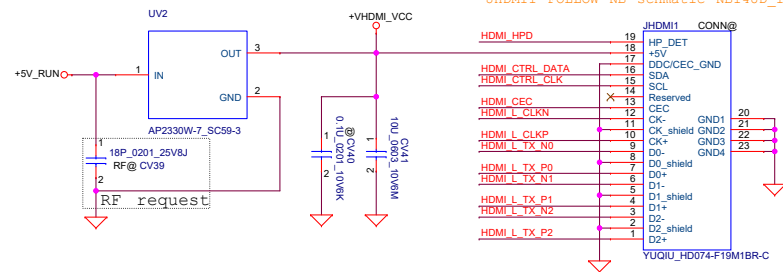
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HDMI connector

JHDMI1 FOLLOW NB schmatic NB14UD 180628



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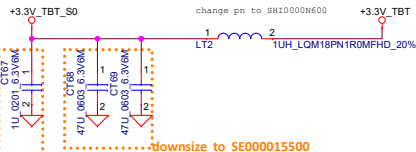
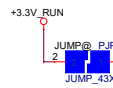


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TBT Power circuit

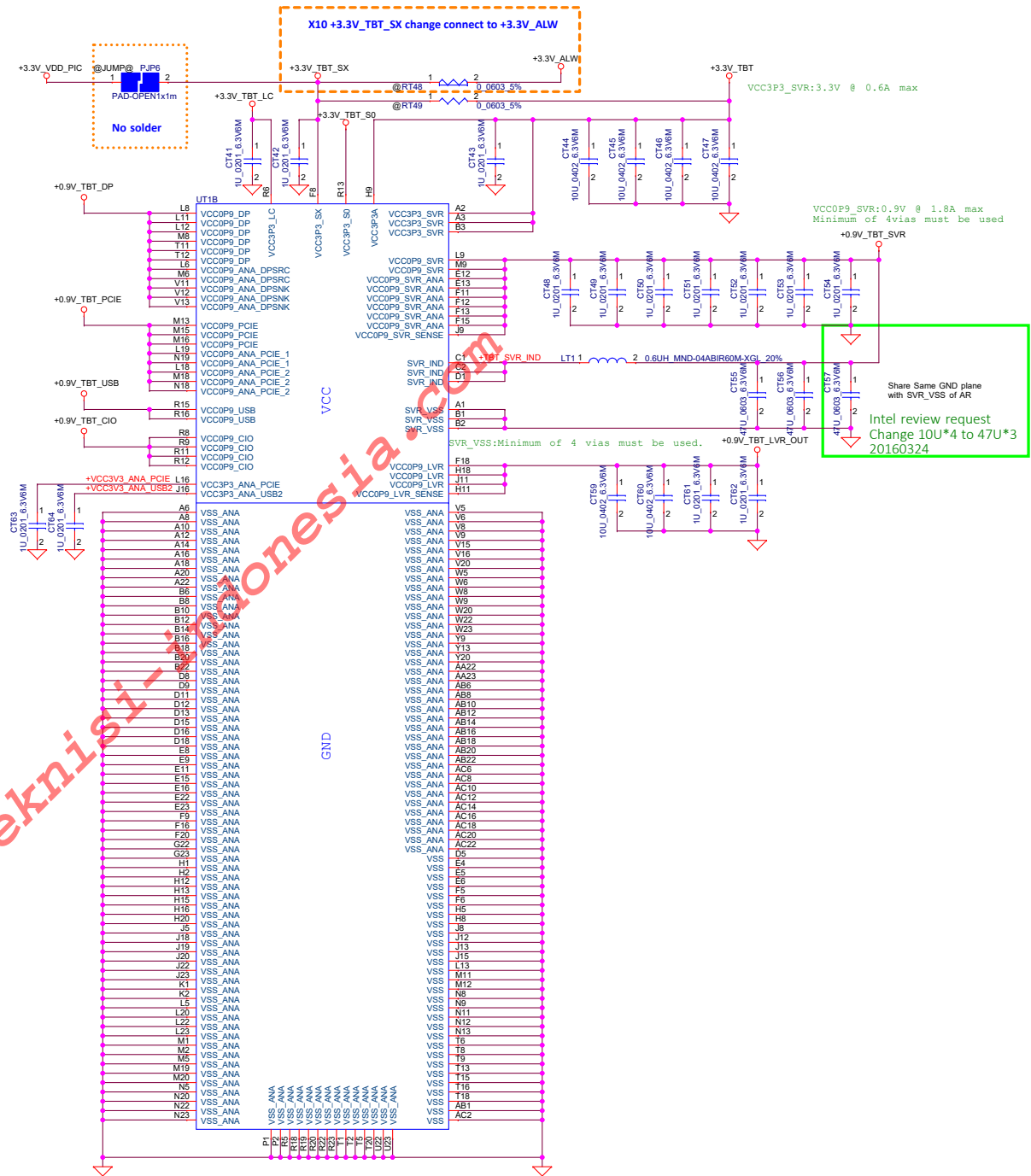


downsize to SE00000UC00

Power Consumption

- Design power plane supports maximum current requirement

VCC3V3_S0_SYS	VCC3V3_TBT_SX	VCC3V3_IC	VCC3V3_ANA_PCIE	VCC3V3_ANA_USB2	
1.05A	0.19A	0.03A	0.1A	0.1A	
VCC0V9_SVR	VCC0V9_LVR_OUT	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
1.83A	0.06A	0.7A	0.58A	0.22A	0.28A



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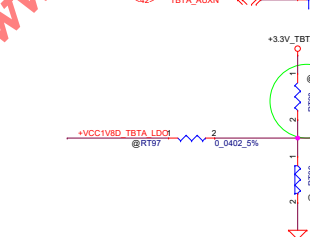
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TBT-AR-SP(2/2) PWR,VSS

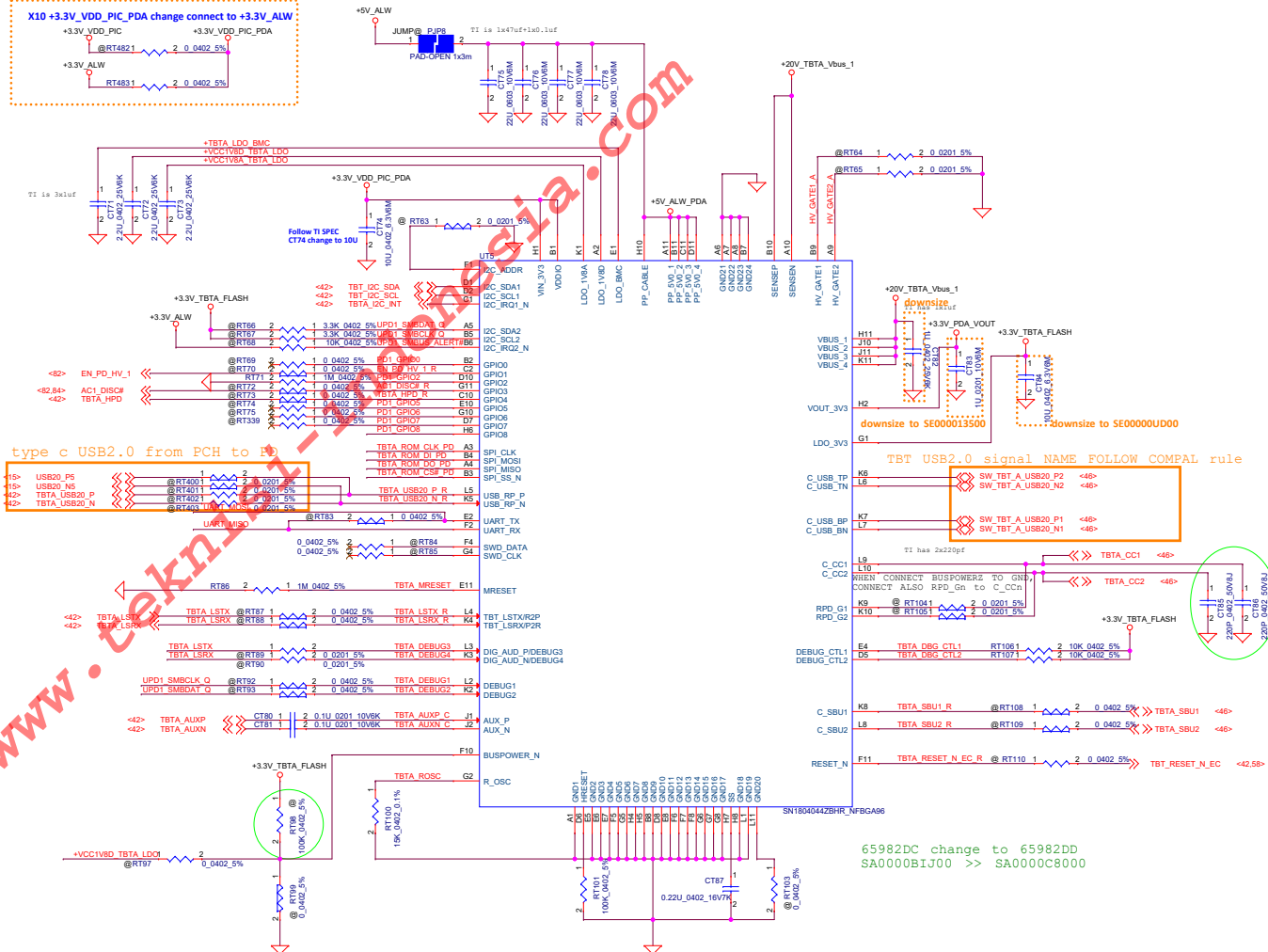
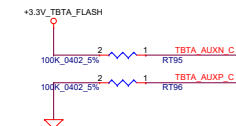
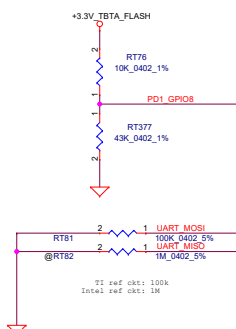
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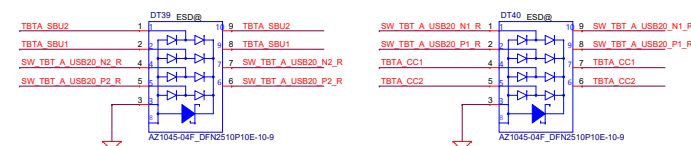
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DIV = R2/(R1+R2)		Factory Configuration	Device Configuration	Description
DIV_min	DIV_max			
0.00	0.08	0		UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1		UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations TI VID supported
0.20	0.28	2		UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3		UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configurations TI VID supported
0.40	0.48	4		DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power swaps, but does not initiate.
0.50	0.58	5		DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap-to UFP and can initiate.
0.60	0.68	6		DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap-to DFP and can initiate.
0.70	1.00	7		Infinite boot retry from Flash to Host IF cycles.



For AR Config



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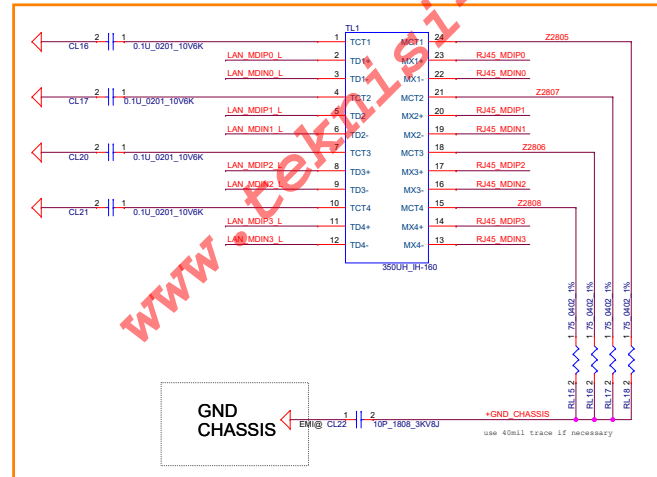
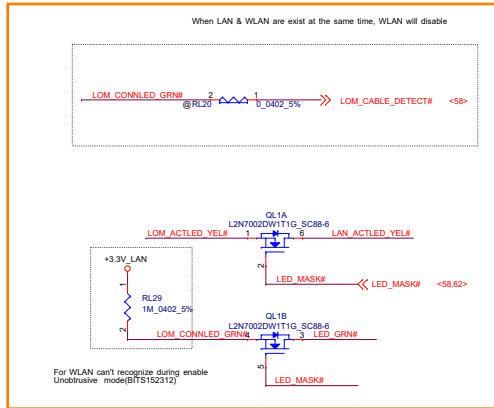
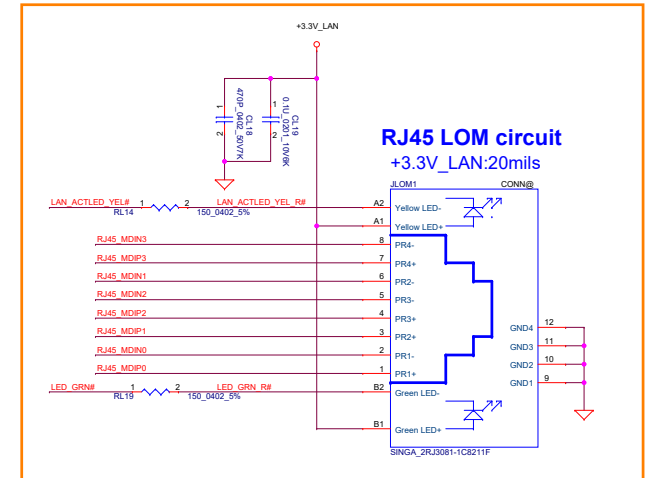
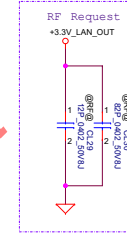
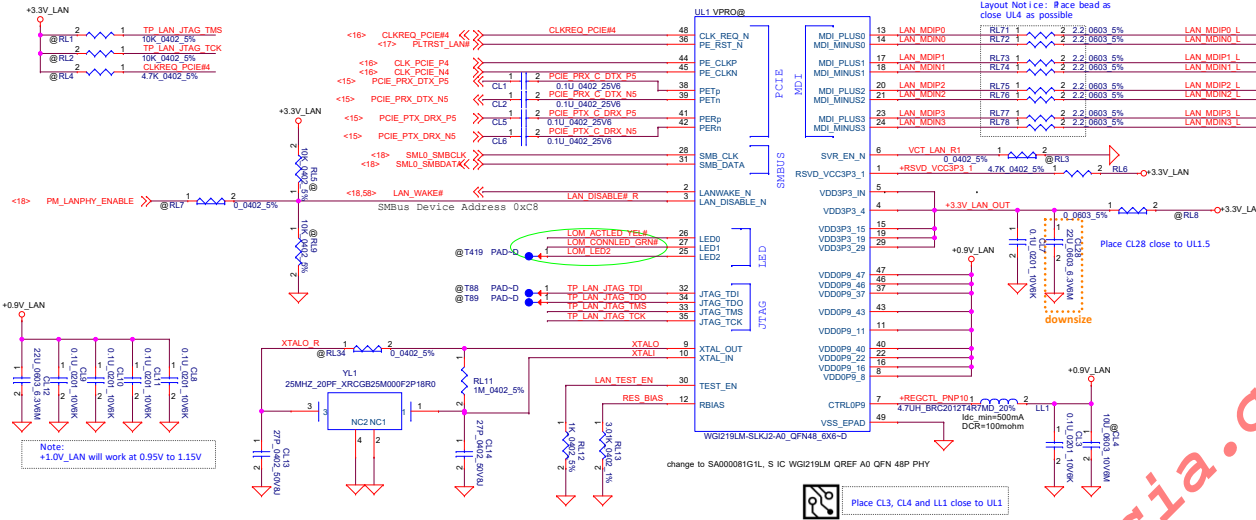
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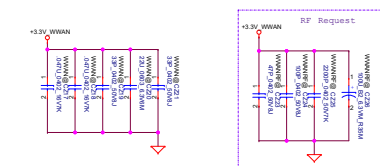
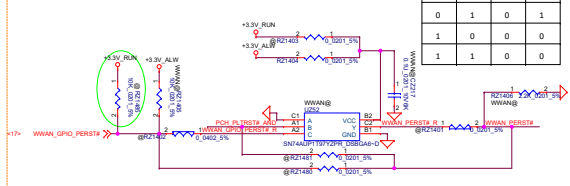
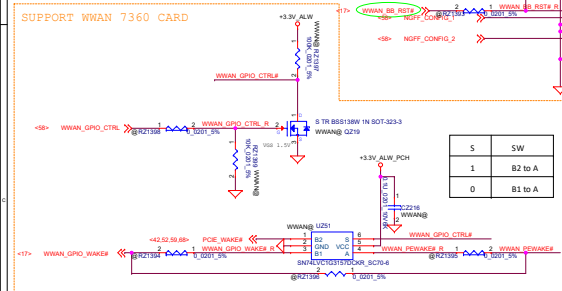
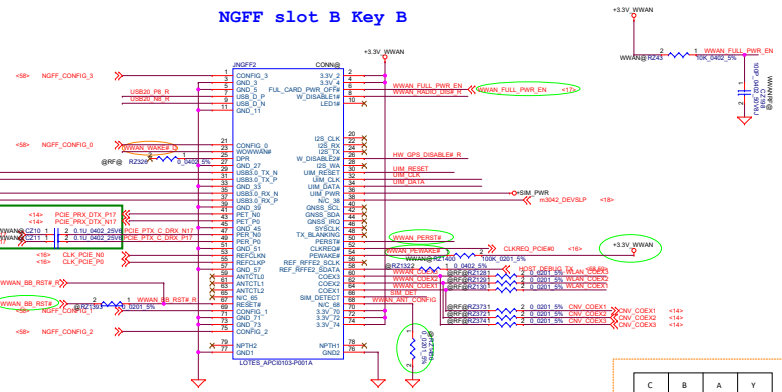
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NVPRO LAN CHIP SA00009340L
NVPRO BOM OPTION IN PAGE 63



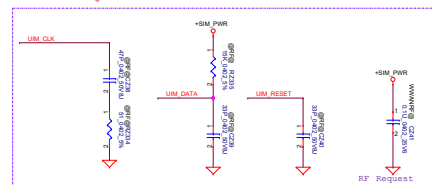
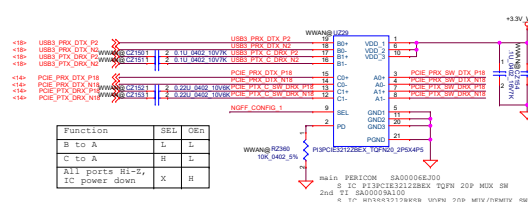
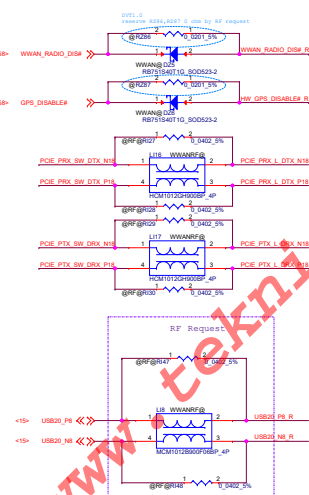
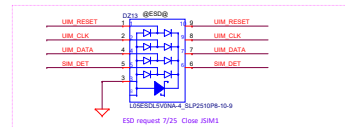
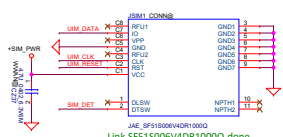
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				LAN Clarkville & RJ45	
Size		Document Number		Rev	
LA-H172P		LA-H172P		0.1	
Date:		Tuesday, March 12, 2019		Sheet 51 of 100	

NGFF slot B Key B

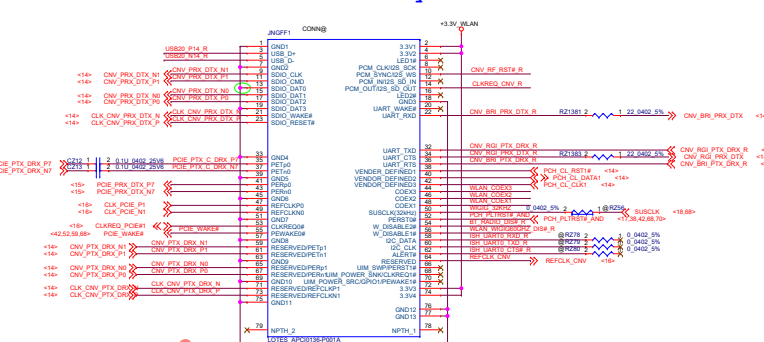


STATE #	CONFIG_0 (PIN#1)	CONFIG_1 (PIN#9)	CONFIG_2 (PIN#1)	CONFIG_3 (PIN#1)	Module Type	m3042_PCIE#_SATA#
0	GND	GND (PEDET_PD)	GND	GND (device_PD)	SSD-SATA	High
1	GND	HIGH (PEDET_NC)	GND	GND	SSD-PCIe(2 lane)	Low
8	GND (device_PD)	GND (device_PD)	HIGH (device_NC)	HIGH (device_NC)	WWAN	Low
	GND (device_PD)	GND (device_PD)	GND (device_NC)	HIGH (device_NC)	WWAN	Low
15	EC MR_P1(1)	EC MR_P1(1)	EC MR_P1(1)	EC MR_P1(1)	NA	Low

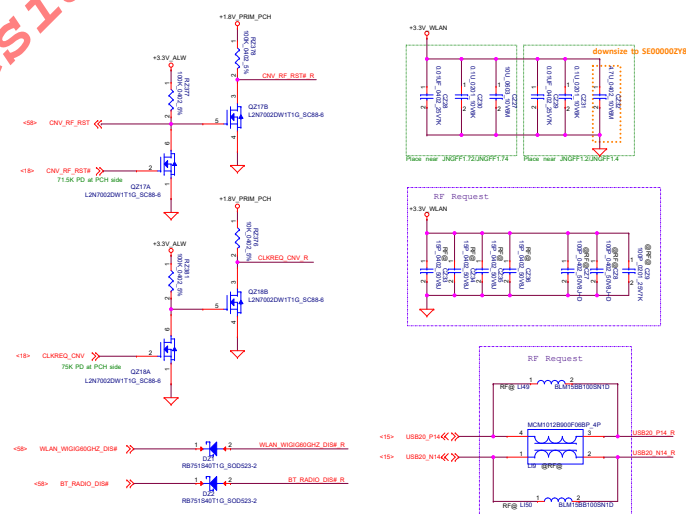
SIM Card Push-Push




NGFF slot E Key E



Link LOTES_APCI0136-P001A done



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Classification		Compul Secprod Data			
Issued Date	2018/01/01	Deciphered Date	2020/01/01	Title	NGFF Card
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Size	Document Number	Rev
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Document Number

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Sheet

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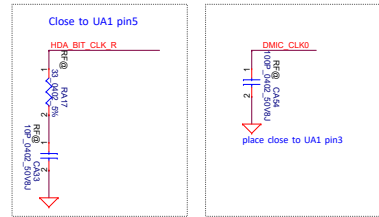
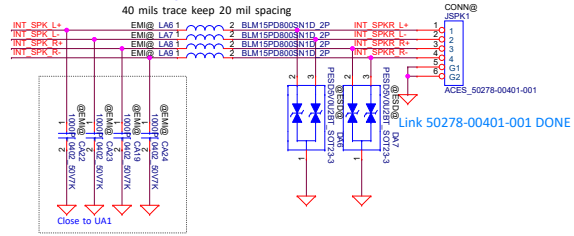
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BH audio codec SUPPORT ALC3204

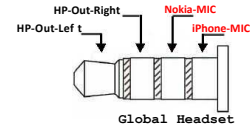
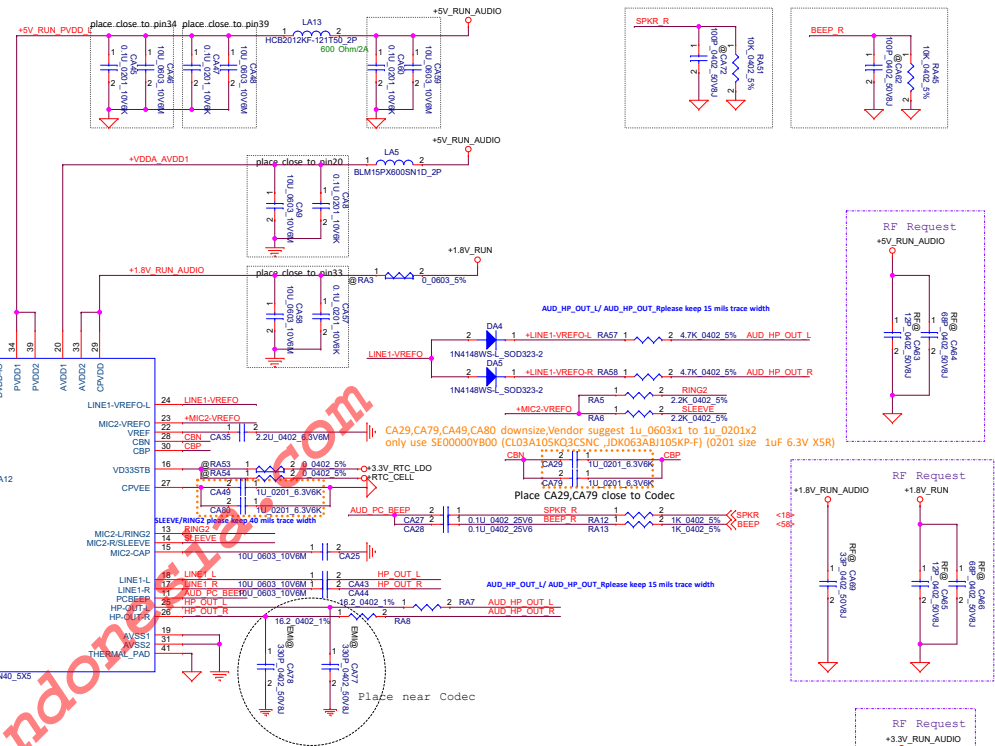
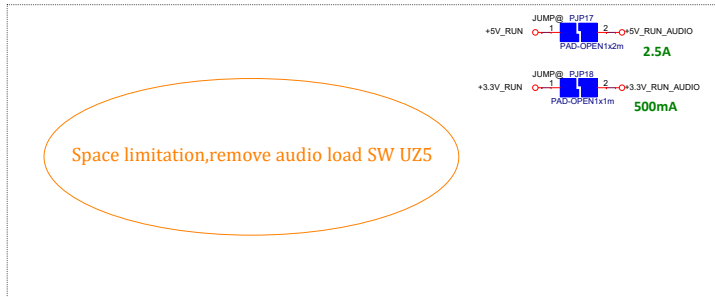
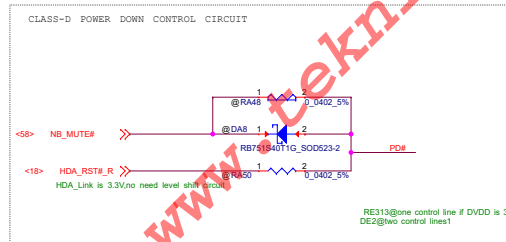
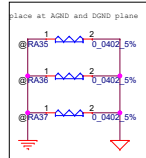
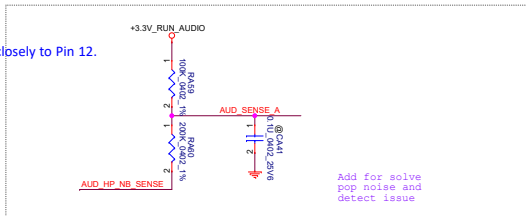
SCHMATIC FOLLOW NB15UD_180605

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

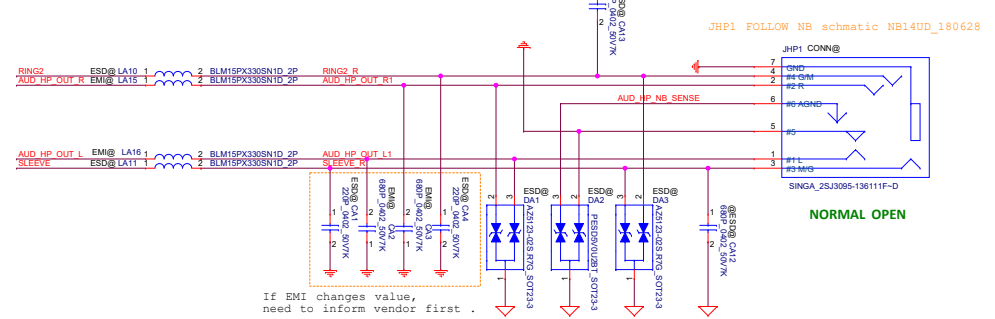
Internal Speakers Header



Place closely to Pin 12.



Universal Jack



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Compal Electronics, Inc.

Codec ALC3204

LA-H171P

Date: Monday, March 11, 2019 Sheet 98 of 100

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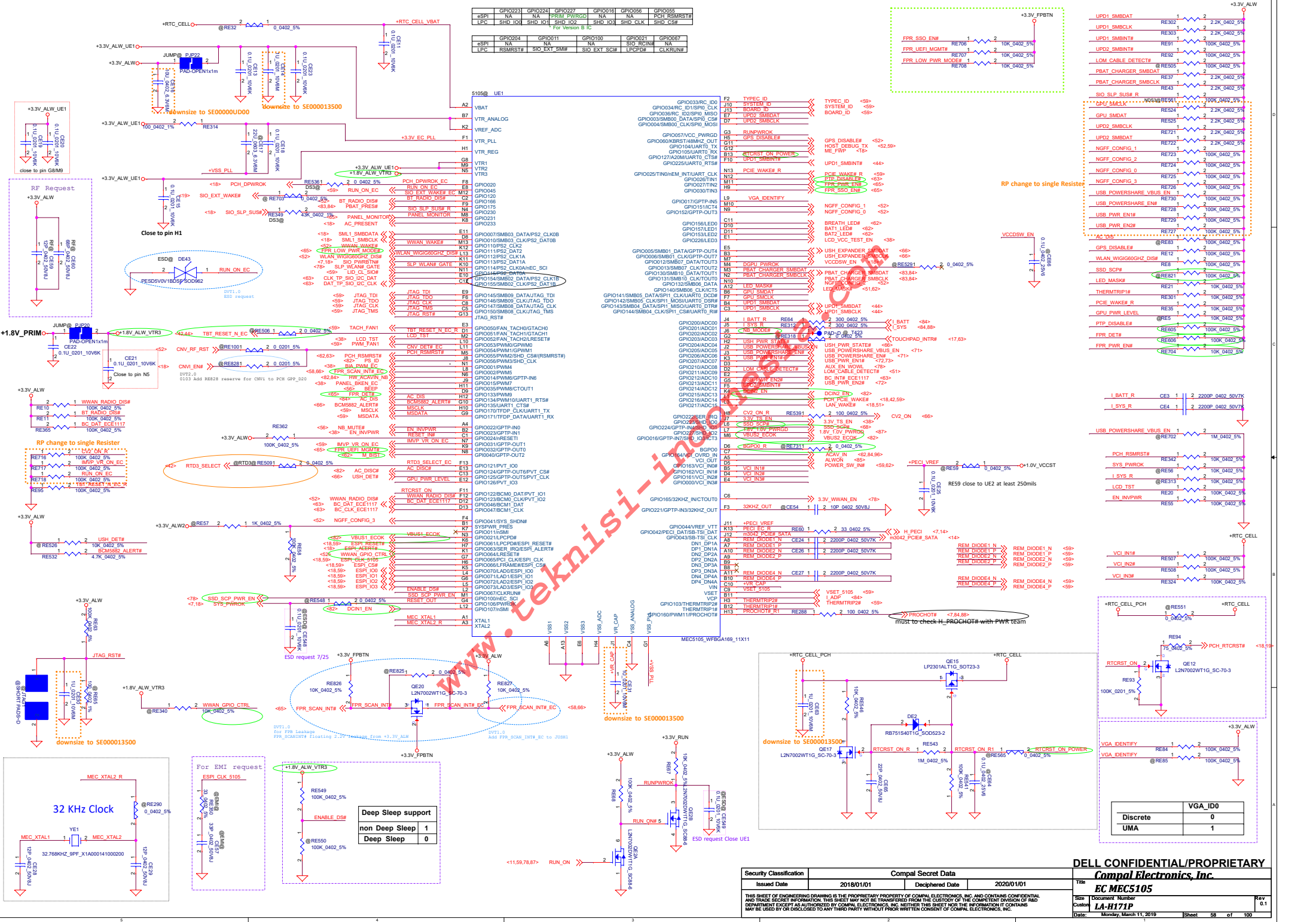
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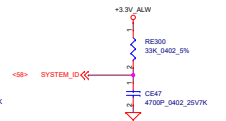
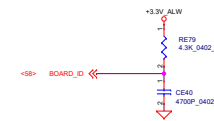
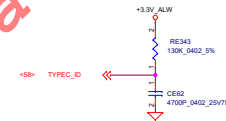
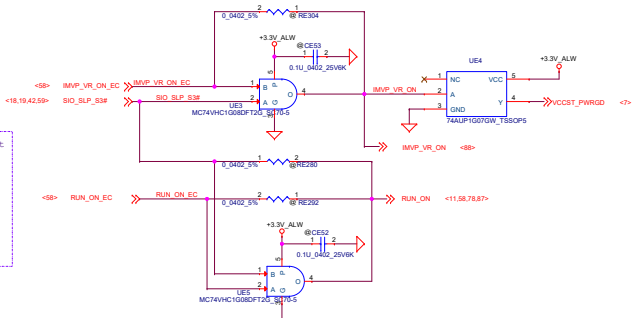
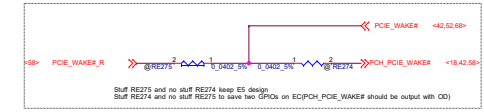
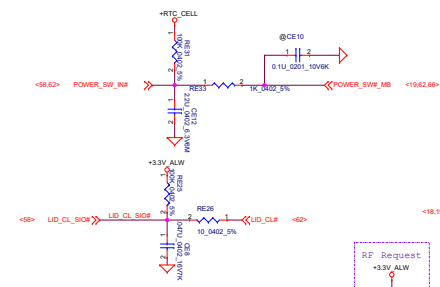
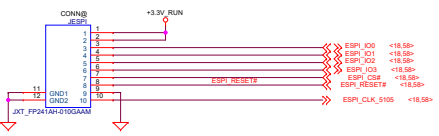
Title		
Audio Ampfilter		
Size	Document Number	Rev
	LA-H171P	0.1
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	RE343	CE62	REV
*	240K	4700p	Single Port ACE w/o AR
	130K	4700p	Single Port ACE w/AR
	62K	4700p	Dual Port ACE w/o AR
	33K	4700p	Dual Port ACE w/AR
	8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
	4.3K	4700p	,
	2K	4700p	
	1K	4700p	

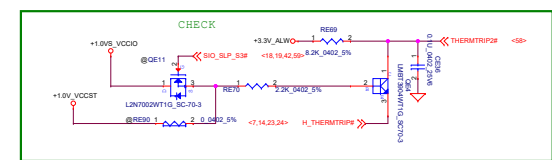
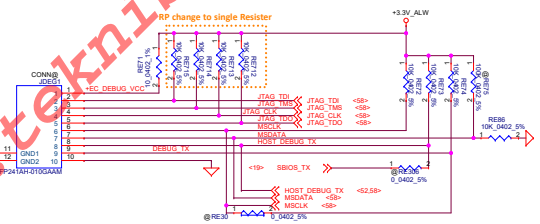
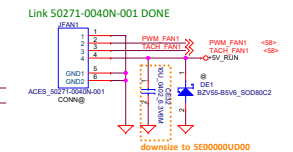
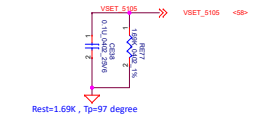
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
8.2K	4700p	BR15 H
4.3K	4700p	17"
2K	4700p	BR15 P
1K	4700p	

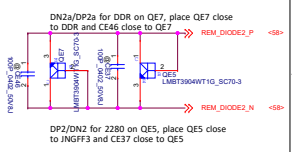
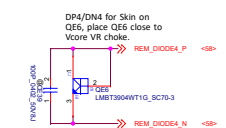
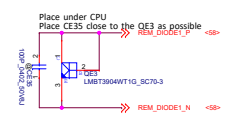
PD_ACE_DET# rise t i n e l s m e a s u r e d f r o m 5 % ~ 68 %

BOARD_ID rise t i n e i s m e a s u r e d f r o m 5 % ~ 68 %

PANEL_ID rise t i n e i s m e a s u r e d f r o m 5 % ~ 68 %



5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	2280 (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



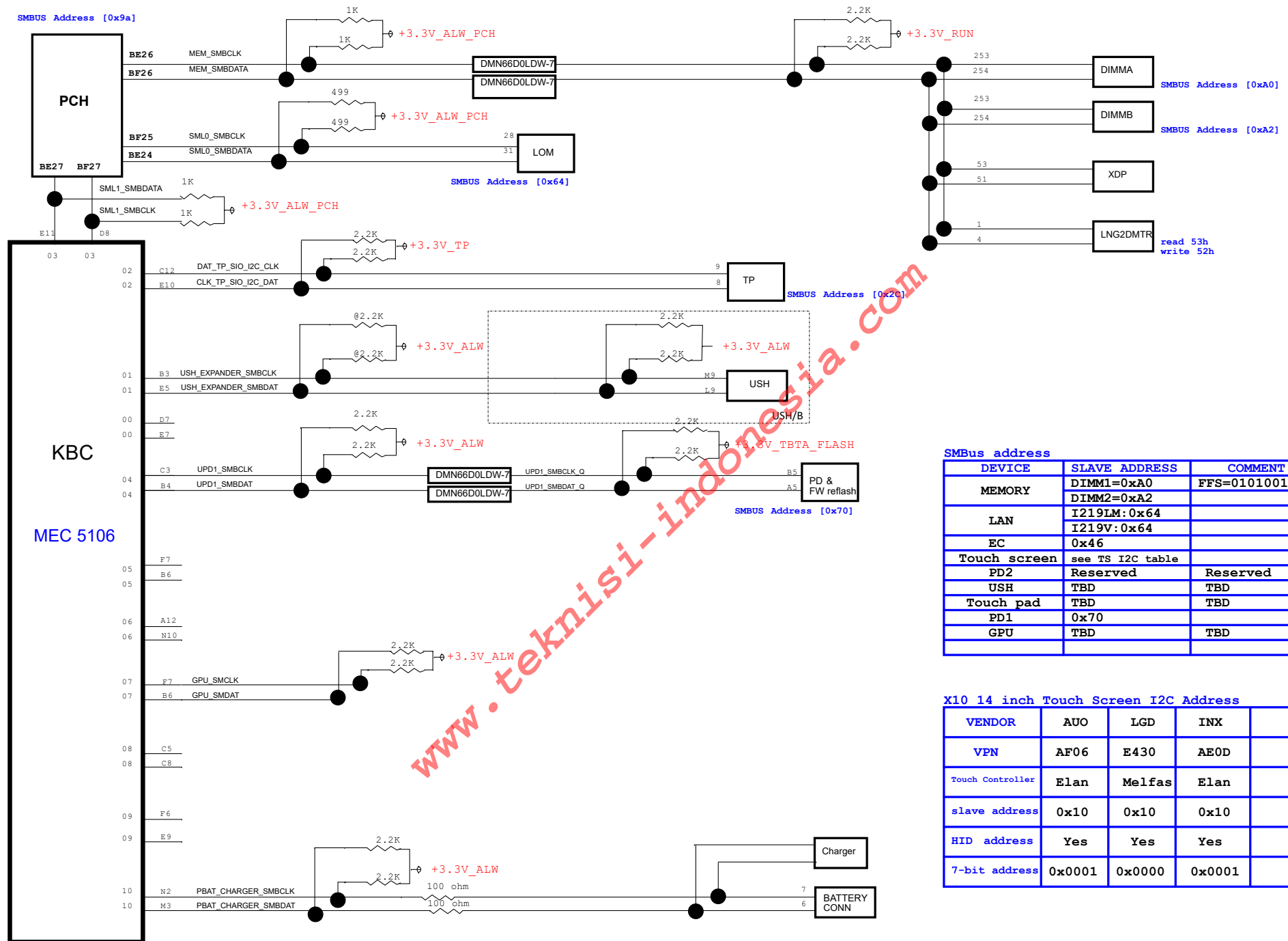
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Secure & Reset IC		
Size	Document Number	Rev
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Date:	Friday, March 08, 2019	Sheet 60 of 100

SMBUS Address [0x9a]

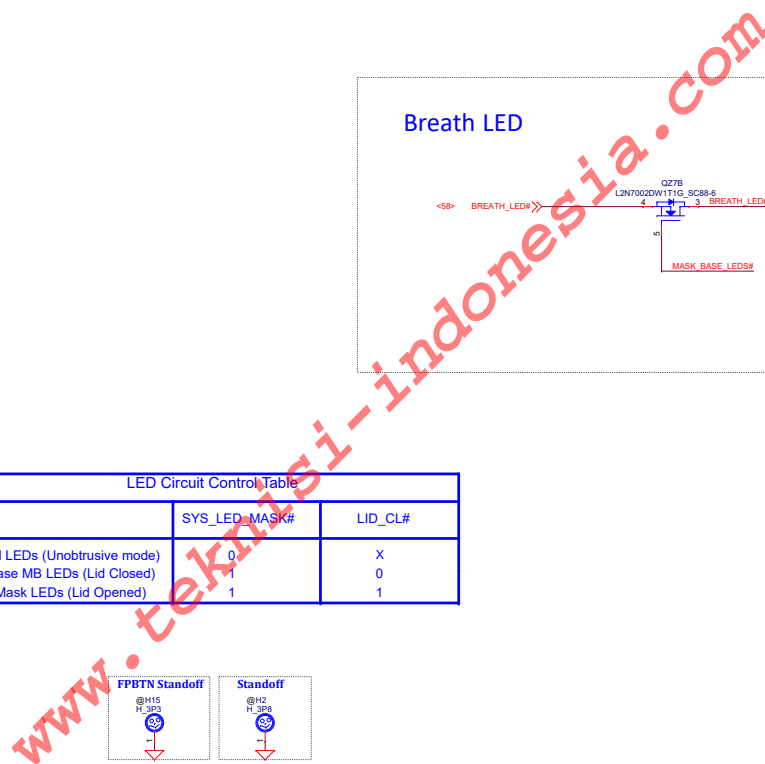
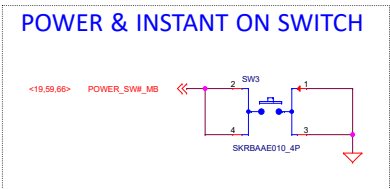


SMBus address

DEVICE	SLAVE ADDRESS	COMMENT
MEMORY	DIMM1=0xA0	FFS=0101001b
	DIMM2=0xA2	
LAN	I219LM:0x64	
	I219V:0x64	
EC	0x46	
Touch screen	see TS I2C table	
PD2	Reserved	Reserved
USH	TBD	TBD
Touch pad	TBD	TBD
PD1	0x70	
GPU	TBD	TBD

X10 14 inch Touch Screen I2C Address

VENDOR	AUO	IGD	INX	
VPN	Af06	E430	AE0D	
Touch Controller	Elan	Melfas	Elan	
slave address	0x10	0x10	0x10	
HID address	Yes	Yes	Yes	
7-bit address	0x0001	0x0000	0x0001	

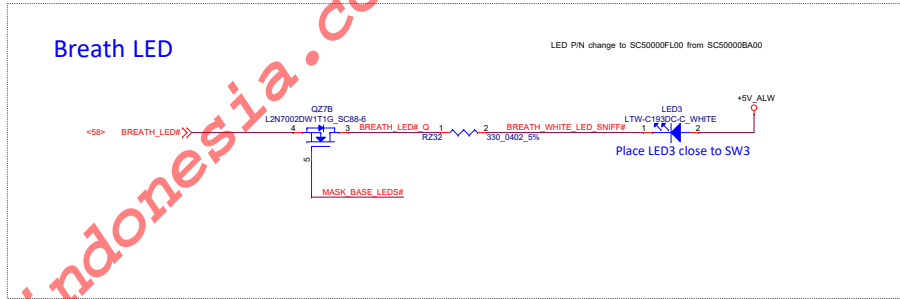
[illegible]

Battery LED

The image shows two circuit diagrams for connecting a Battery LED. Each diagram consists of a horizontal red line representing a wire. On the left, a red arrow points to the wire, labeled with a pin number and a label in red. On the right, a red arrow points away from the wire, labeled with a pin number and a label in red. In the middle, a resistor is connected between the wire and ground. The resistor is represented by a zigzag line with the value '150_0402_5%' written below it. The ground symbol is a horizontal line with three diagonal lines of decreasing length.

<S8> BATT2_LED# 1 2 150_0402_5% BATT_WHITE#

<S8> BATT1_LED# 1 2 330_0402_5% BATT_YELLOW#



The diagram shows the connection for the LED board. The JLED1 connector has 8 pins. The connections are as follows:

- Pin 1: +3.3V_ALW
- Pin 2: LID_CL#
- Pin 3: BATT_WHITE#
- Pin 4: BATT_YELLOW#
- Pin 5: +5V_ALW
- Pin 6: Ground
- Pin 7: GND1
- Pin 8: GND2

The bottom of the diagram shows the HRS_TF31-6S-0P5SH connector with pins 1 through 5, and a note "CONN@".

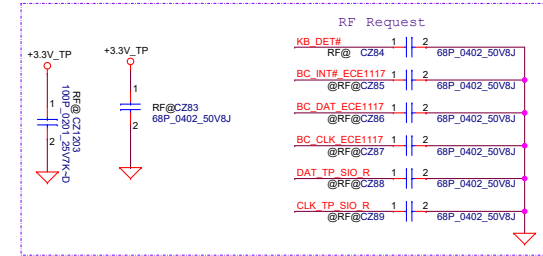
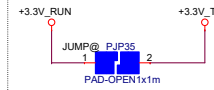
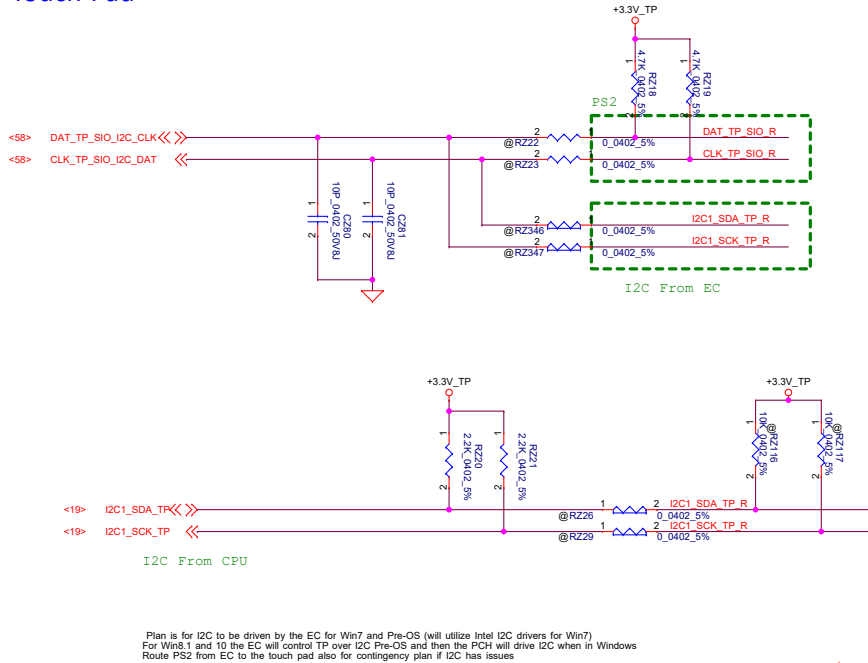
AR crystal shielding can

The diagram shows a blue rectangular component labeled 'P1' with 'SI0N_C7521R' written below it. To the left of the component is a red arrow pointing left, labeled '1'. Above the component are the labels 'SHDCAN' and 'CONN@'.

AR,PD clip

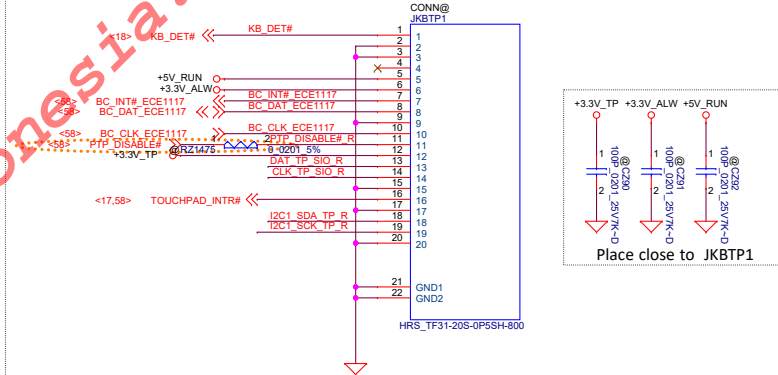
The diagram shows four identical blue rectangular components labeled 'P1' arranged horizontally. Each component has 'EMIST_SUL-12A2M_1P' written below it. To the left of each component is a red arrow pointing left, labeled '1'. Above each component are the labels 'CLP1 CONN@', 'CLP2 CONN@', 'CLP4 CONN@', and 'CLP3 CONN@' respectively.

Touch Pad

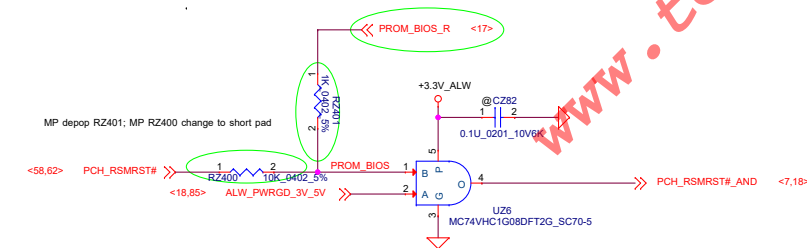


JKBTP1 FOLLOW NB schmatic NB15UD_180628

Keyboard



RSMRST circuit



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Title		
Reserve for KB/TP/LED/LID		
Size	Document Number	Rev
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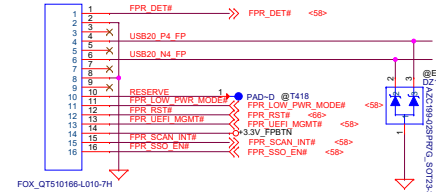
BH SUPPORT FPR in Power BUTTON SCHEMATIC FOLLOW NB15UD_180605

FP in PWR BUTTON connector

FP IN BTN USB2.0 need check port map

NEED check EC GPIO TABLE

CONN@_JFPBTN1



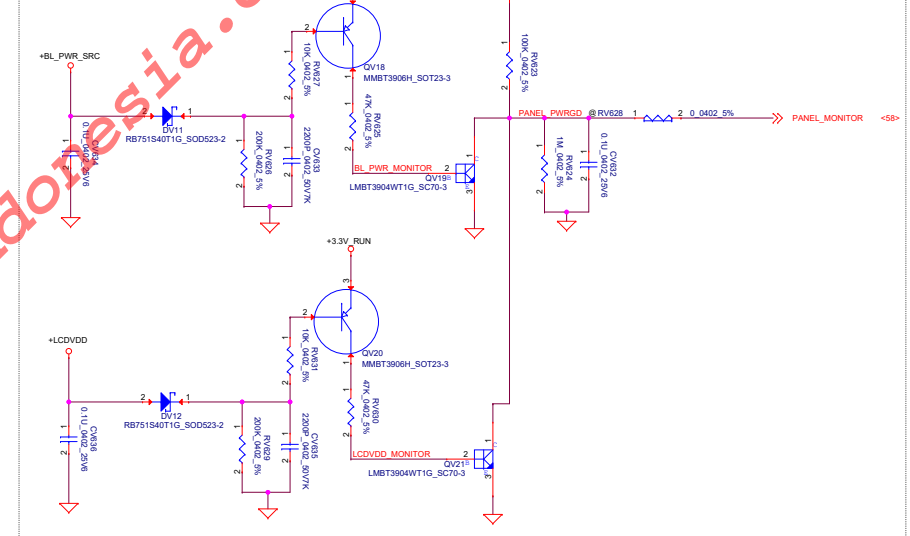
Link FOX_QT510166-L010-7H done

Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR_DET(GND)	16

9/26 ESD Request



For BL_PWR_SRC & LCDVDD monitor



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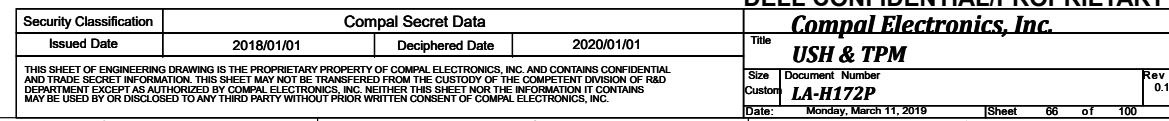
Compal Electronics, Inc.

FP in PWRBTN

LA-H172P
Date: Monday, March 11, 2019 Sheet 65 of 100

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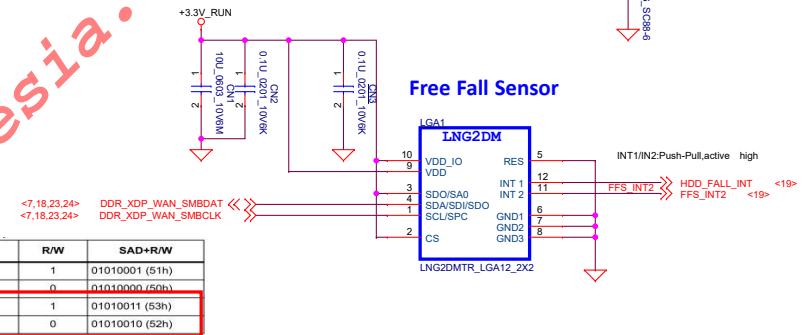
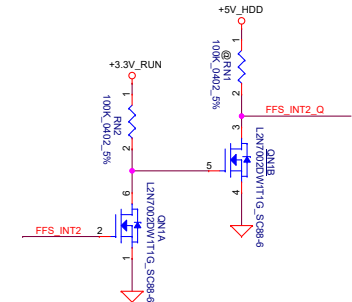
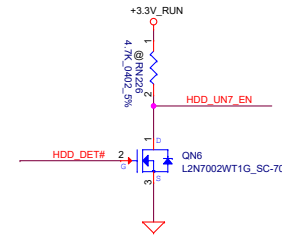
BH USH/B SUPPORT CV3
SCHEMATIC FOLLOW NB15UD_180605



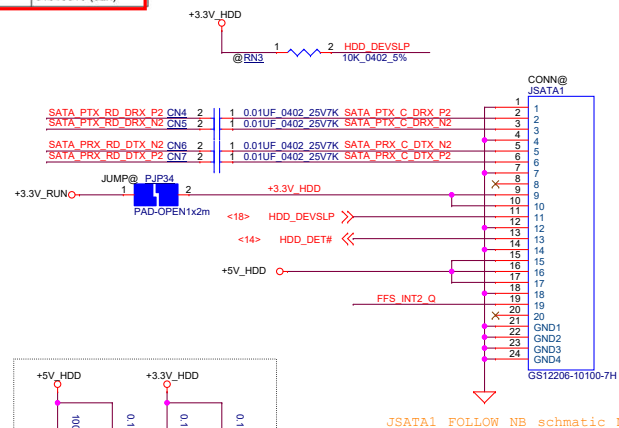
18,19,66,87> SIO_SLP_S0# >> 1 2 HDD_UN7 EN_R
RB751S40T1G_SOD523-2
@DN1
DWT1.0
for save power consumption
reserve Dn1 connect to SIO_SLP_S0#

	HDD UN7 EN		2	HDD UN7 EN R7	A _{EM}	B _{EM}	18	HDD A _{EQ2}
N12	1	0.01Uf 0402 25V7K	SATA_PTX_C RD DRX P21	0.0402 5V7K	TdEt _{EM}			
N13	1	0.01Uf 0402 25V7K	SATA_PTX_C RD DRX P22				15	SATA_PTX RD DRX P
N14	1	0.01Uf 0402 25V7K	SATA_PTX_C RD DRX P22				14	SATA_PTX RD DRX P
N15	1	0.01Uf 0402 25V7K	SATA_PTX_C RD DRX P22				12	SATA_PTX RD DRX P
N15	1	0.01Uf 0402 25V7K	SATA_PTX_C RD DRX P22				11	SATA_PTX RD DRX P

			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	A_EQ 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	B_EQ 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	 0 M 1	A_EM 0dB -3.5dB -6dB	B_EM 0dB -3.5dB -6dB



Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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Issued Date	2018/01/01	Deciphered Date	2020/01/01
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Place close JNGFF3 pin 12,14,18

+3.3V_HDD_M2

CN83
0.1uF 0.002 10V7K
0.01uF 0.002 10V7K

Place close JNGFF3 pin 2,4

+3.3V_HDD_M2

CN84
0.1uF 0.002 10V7K
0.01uF 0.002 10V7K

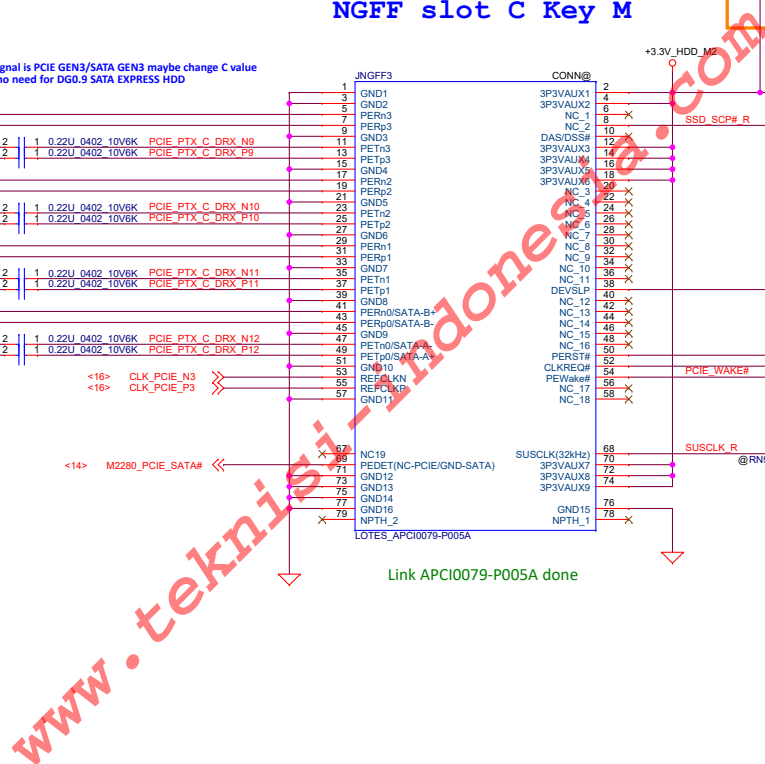
Place close JNGFF3 pin 70,72,74

+3.3V_HDD_M2

CN87
0.1uF 0.002 10V7K
0.01uF 0.002 10V7K

2280 SSD

NGFF slot C Key M

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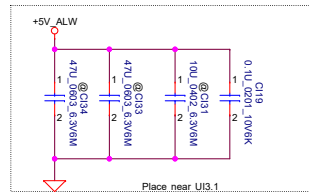
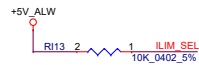
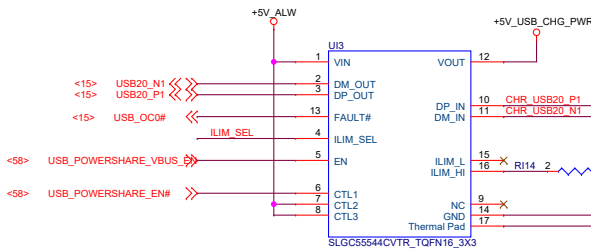
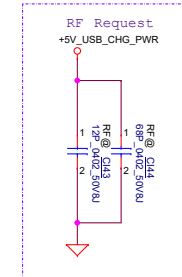
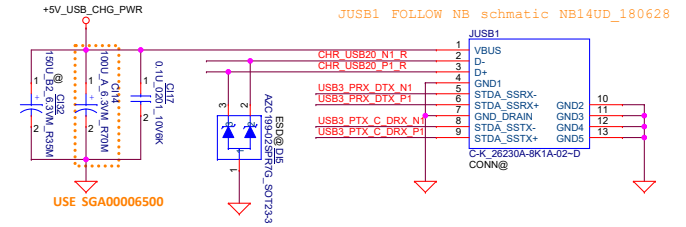
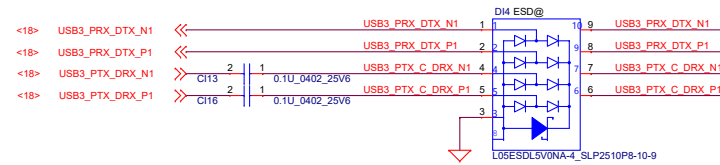
Reserve

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Compal Electronics, Inc.		
Title		
eMMC / UFS		
Size	Document Number	Rev
	LA-H171P	0.1
Date:	Friday, March 08, 2019	Sheet 69 of 100

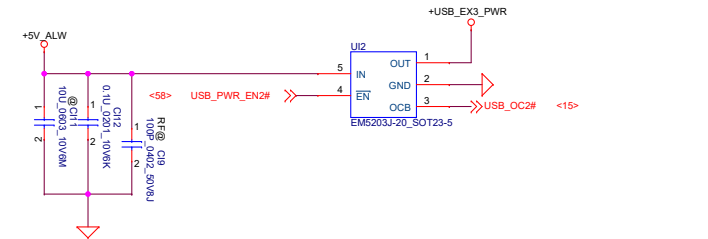
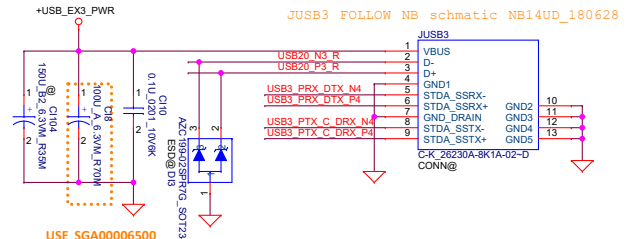
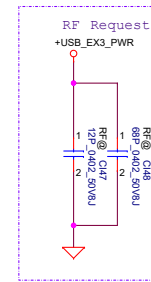
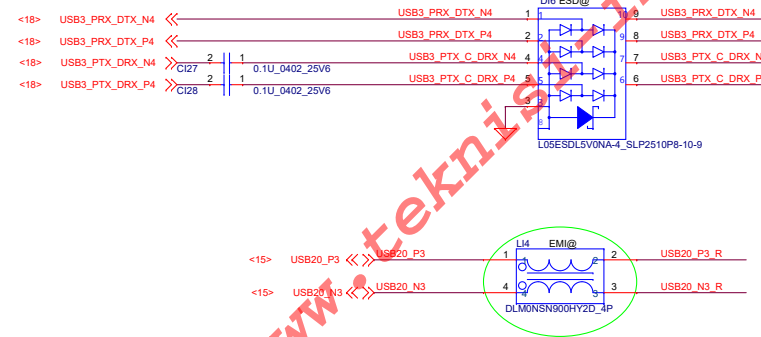
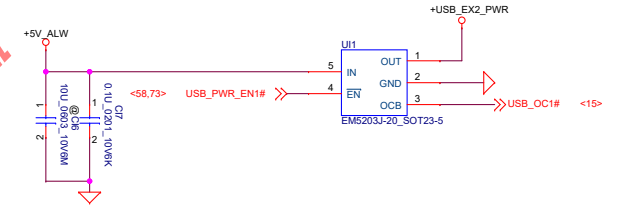
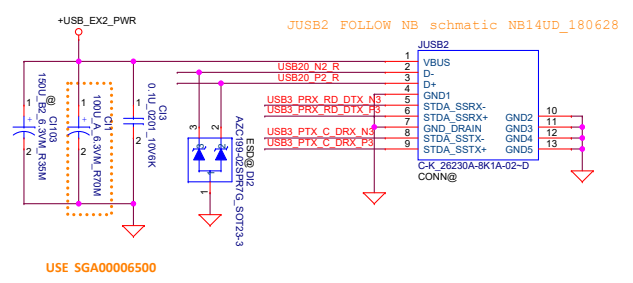
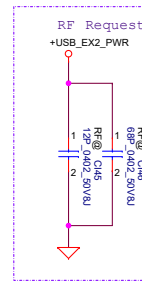
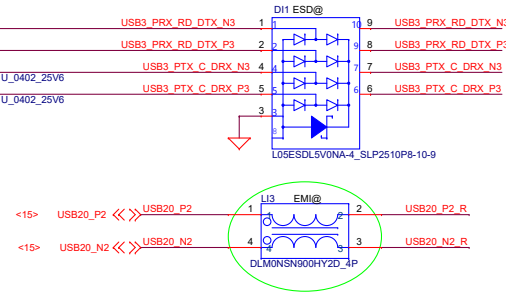
For PWR SW + Charger combine IC



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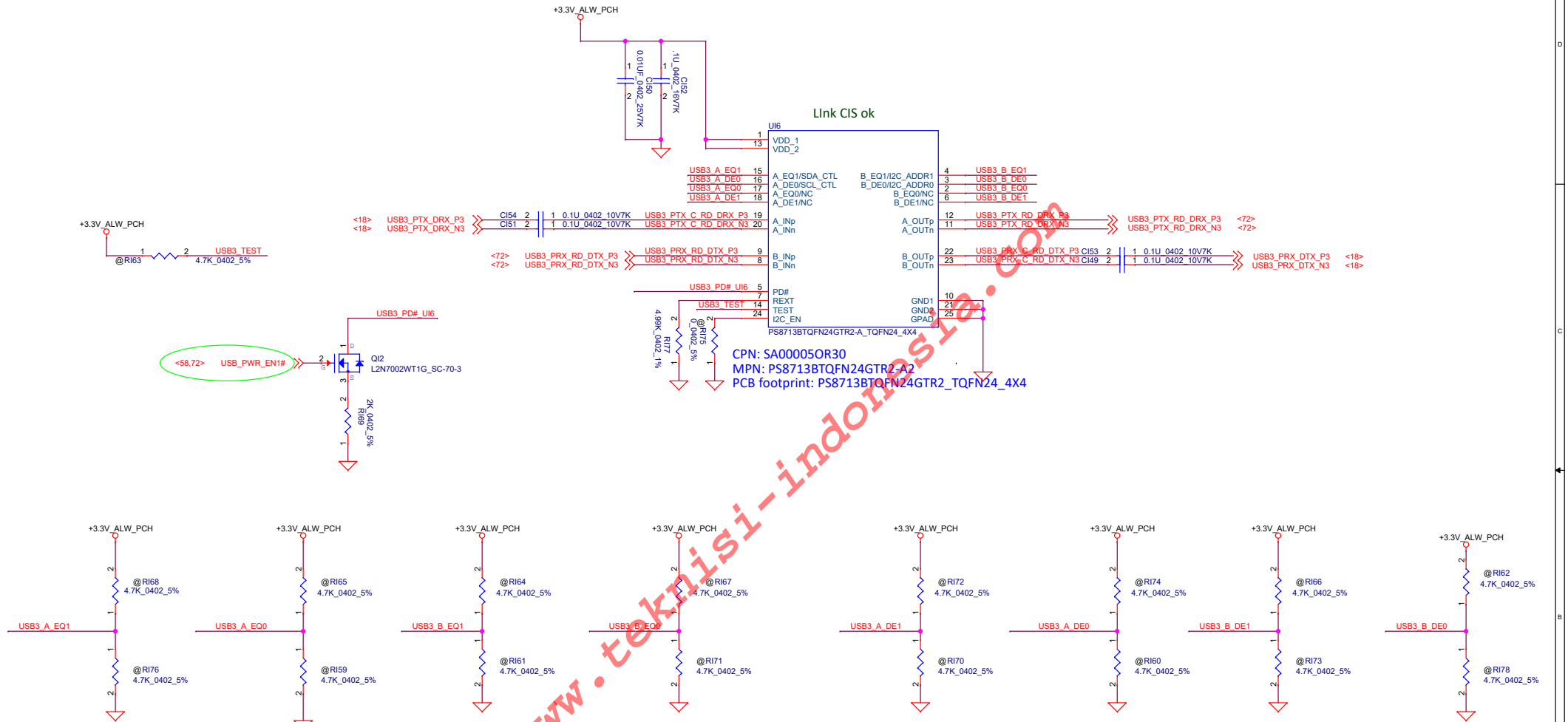
Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				2018/01/01				Compal Electronics, Inc.			
Deciphered Date				2020/01/01				USB SW			
Document Number				LA-H171P				Rev 0.1			
Date:				Monday, March 11, 2019				Sheet 71 of 100			

connect to repeater PS8713



BH USB3.0 add repeater PS8713
SCHMATIC FOLLOW BRMLK14UD_20180316 P.47

FOR LEFT JUSB2 USE



Parade_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A_EQ&B_EQ have internal pull-down 150k

Both A_DE&B_DE have internal pull-down 150k

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Issued Date	2018/01/01	Deciphered Date	2020/01/01
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Compal Electronics, Inc.			
USB3.0 Repeater for JUSB3			
Title	Document Number	Rev	
LA-H171P		0.1	
Date	Friday, March 08, 2019	Sheet	73 of 100

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Compal Electronics, Inc.		
Title		
Dock		
Size	Document Number	Rev
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Date:	Friday, March 08, 2019	Sheet 75 of 100	

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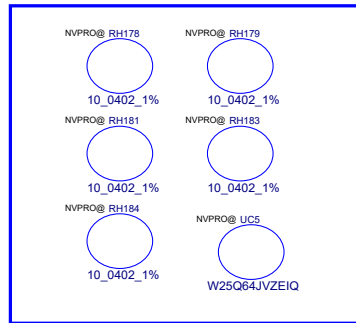


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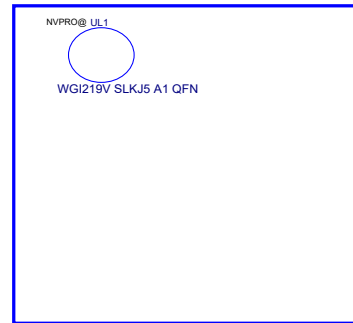
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Title			
Reserve for USB			
Size	Document Number		Rev 0.1
LA-H171P			
Date: Friday, March 08, 2019	Sheet	76 of 100	

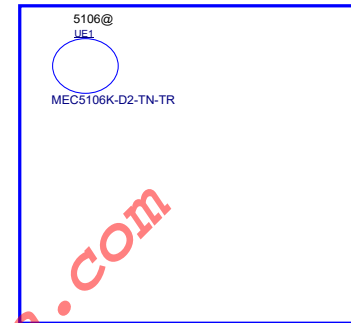
FOR NVPRO ROM BOM OPTION



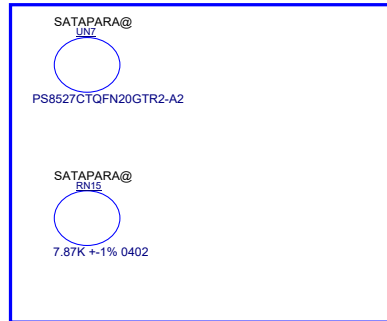
FOR NVPRO LAN chip BOM OPTION



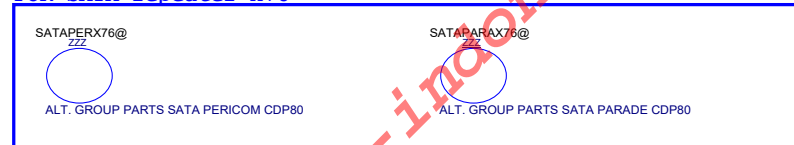
FOR EC MEC5106 BOM OPTION



FOR SATA repeater BOM OPTION



FOR SATA repeater X76



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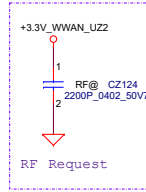
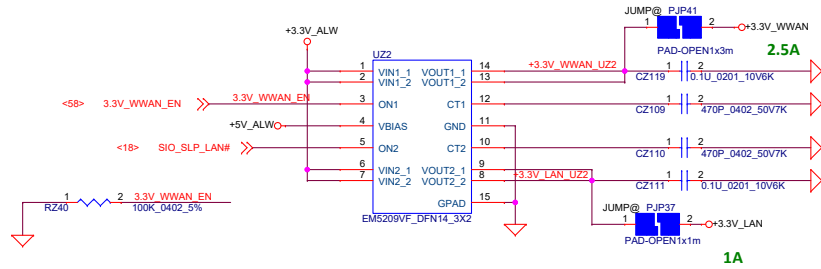
Compal Electronics, Inc.



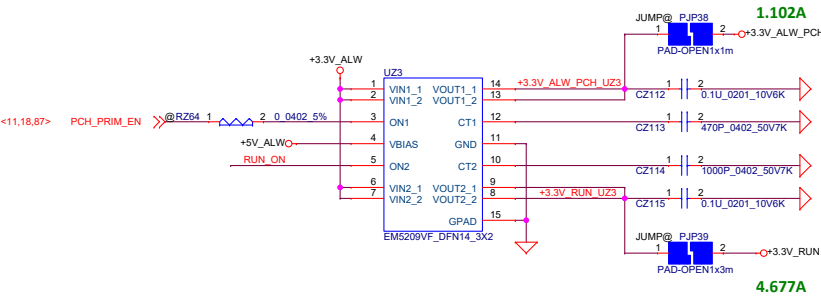
Title			
Bom option			
Size	Document Number		Rev
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Date:	Friday, March 08, 2019	Sheet 77 of 100	

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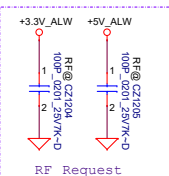
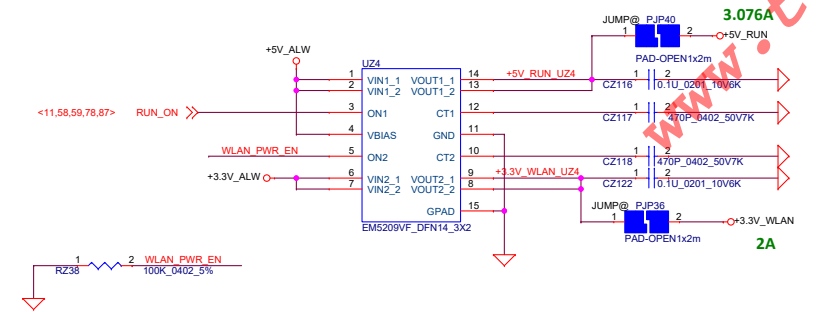
+3.3V_WWAN/+3.3V_LAN source



+3.3V_ALW_PCH/+3.3V_RUN source

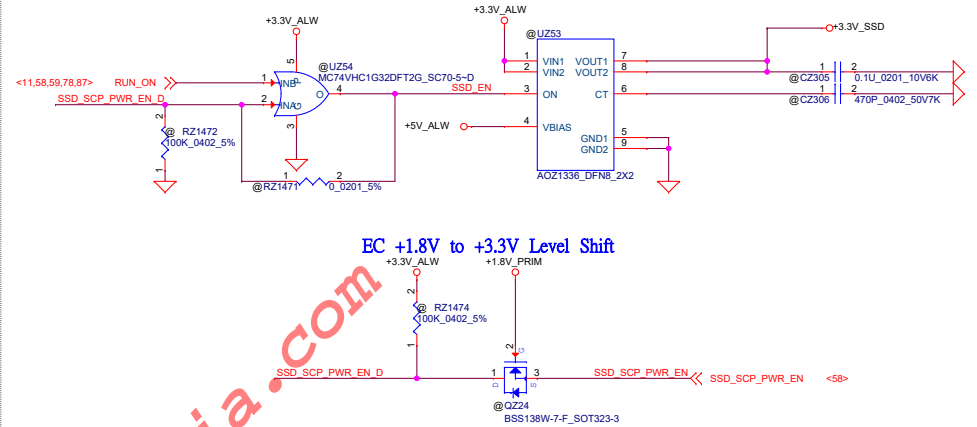


+5V_RUN/+3.3V_WLAN source

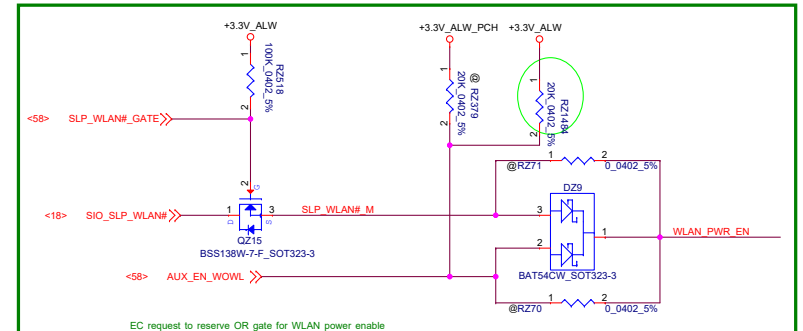
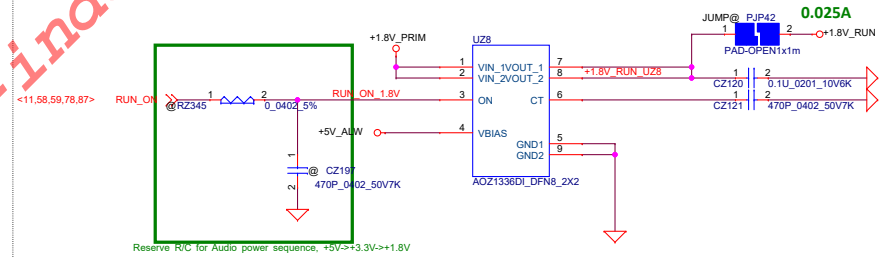


Reserve for SSD storage protection power gate control

SCHMATIC FOLLOW NB15UD_180605



+1.8V_RUN source



Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
Issued Date				Deciphered Date				Compal Electronics, Inc.			
2018/01/01				2020/01/01				Power control			
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				Size B				LA-H171P			
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Reserve for XDP/CMC/APS			
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Title		
Google Debug & INAs		
Size	Document Number	Rev
	LA-H171P	0.1
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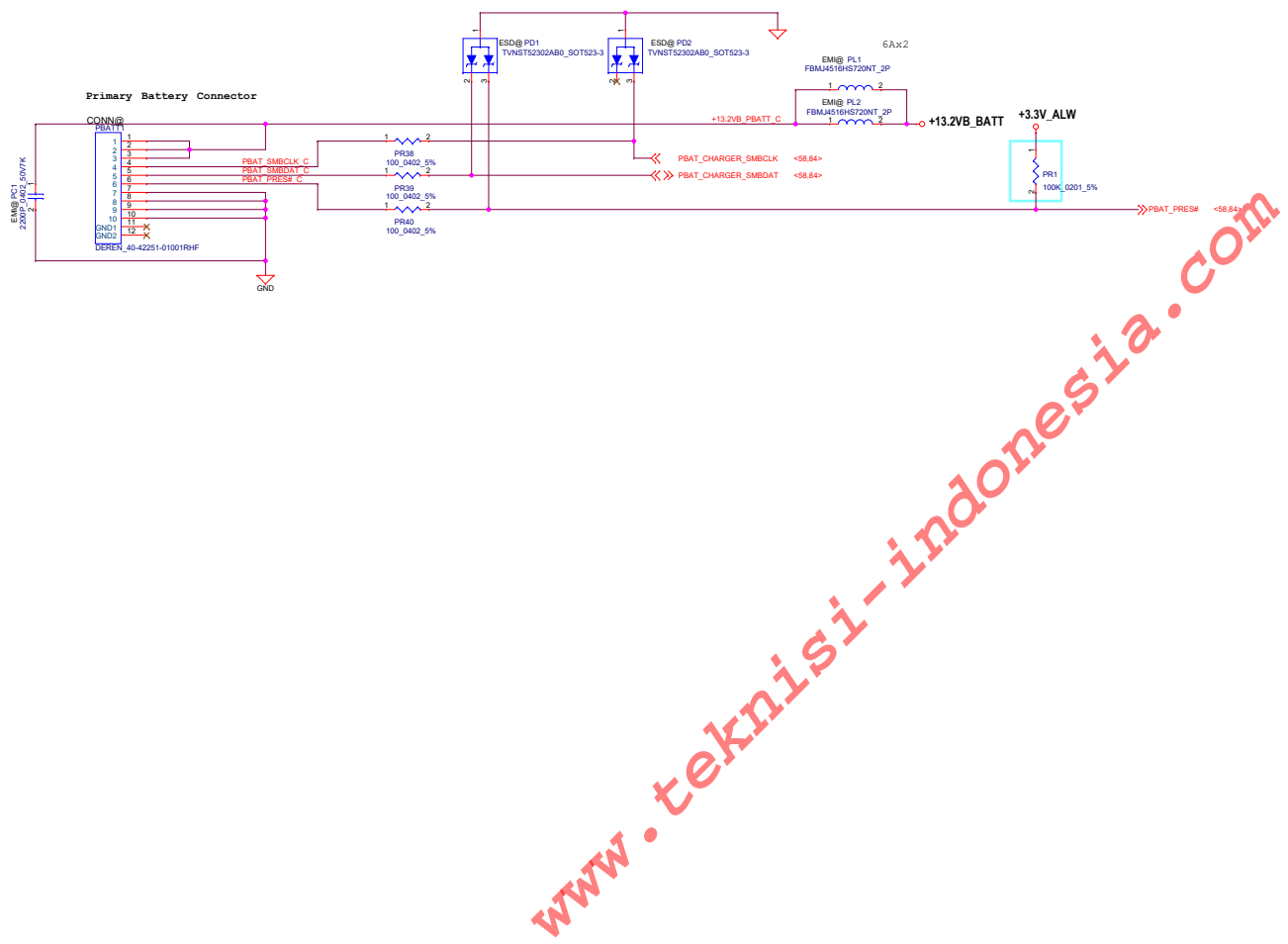
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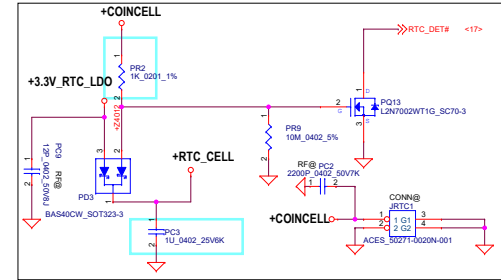
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File		PWR-Block Diagram	
Size	Document Number	Rev	
	DB-2283P	0.1	
Date: Friday, March 08, 2019		Sheet	81 of 101

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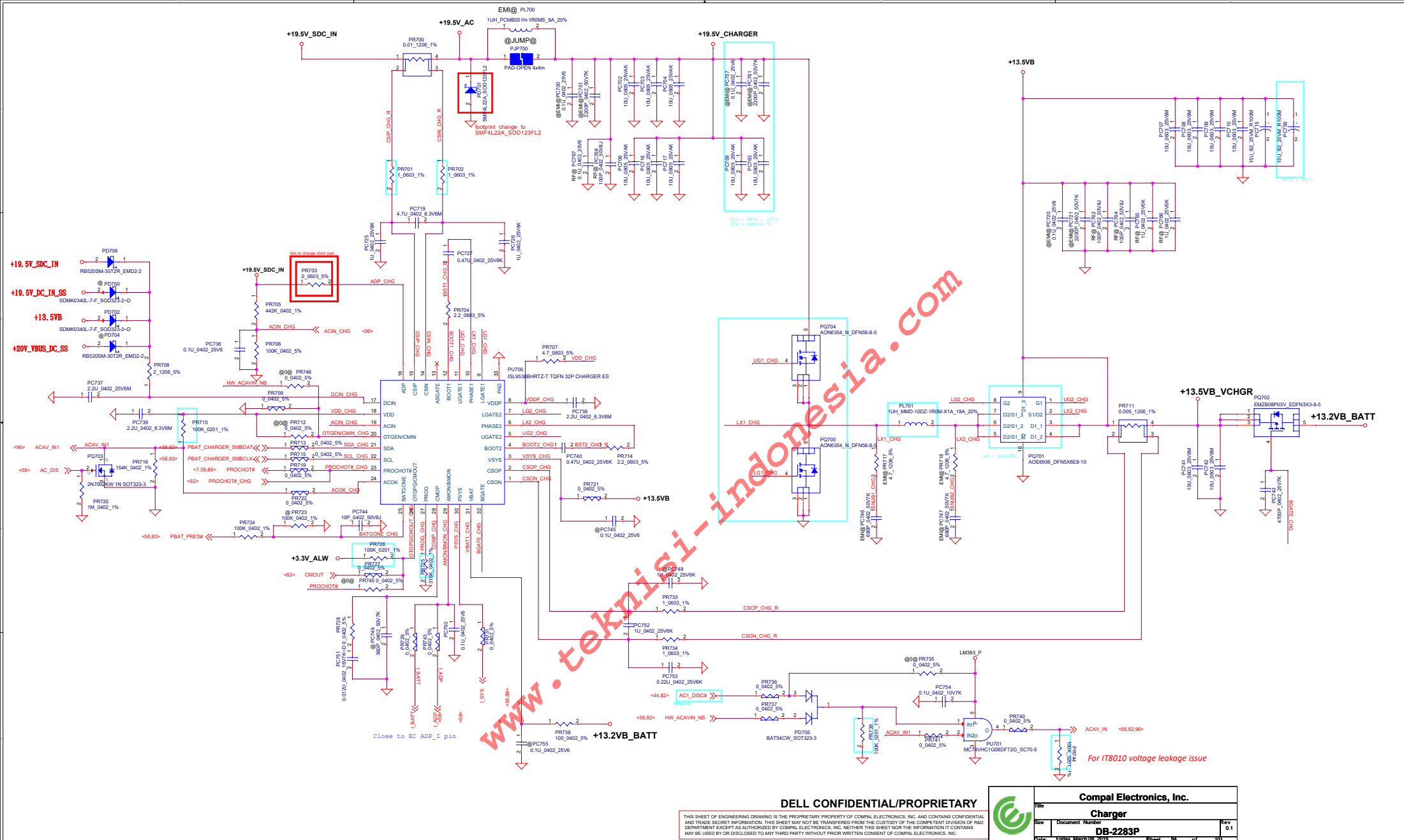
COIN RTC Battery



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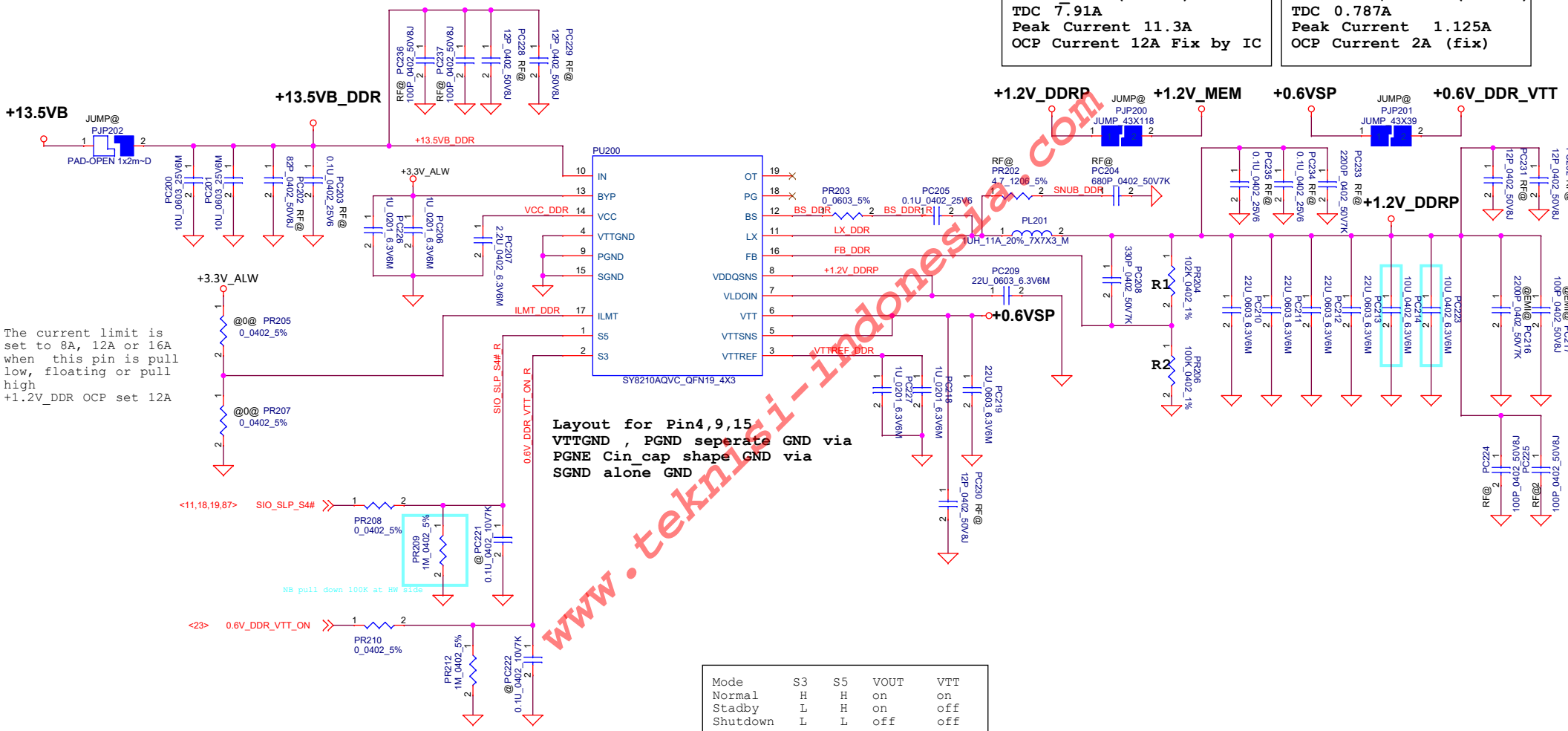
		Compal Electronics, Inc.	
Battery Connector/ RTC		DB-2283P	
Date:	Friday, March 08, 2019	Sheet:	83 of 101

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The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 12A


Layout for Pin4,9,15
VTTGND , PGND separete GND via
PGNE Cin_cap shape GND via
SGND alone GND

+1.2V DDR (1.212V) TDC 7.91A Peak Current 11.3A OCP Current 12A Fix by IC	0.6Volt +/- 5% (0.606V) TDC 0.787A Peak Current 1.125A OCP Current 2A (fix)
---	---

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

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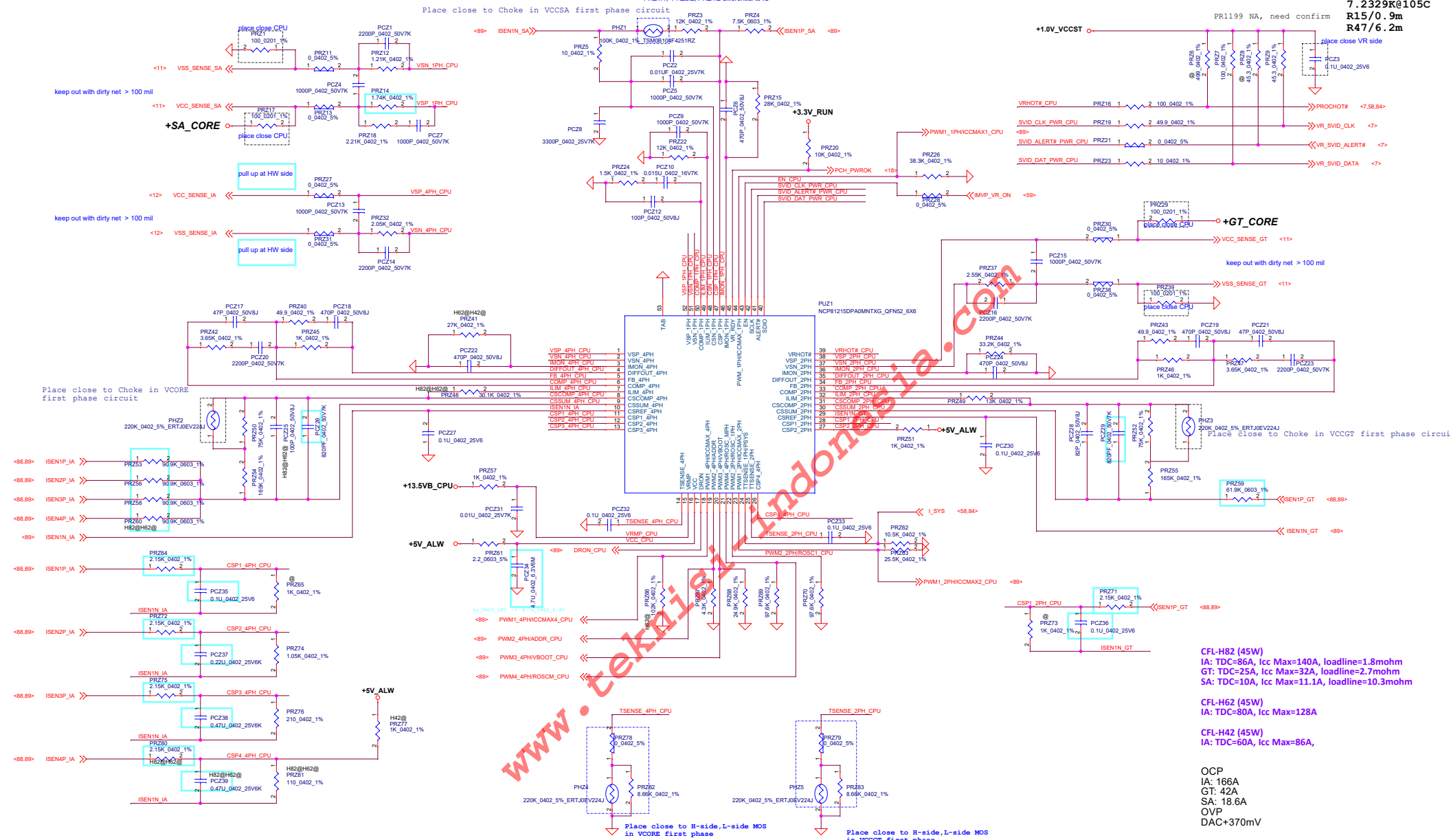
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Title: **+1.2V MEN/+0.6V_DDR_VTT**

Size	Document Number	Rev
	DB-2283P	0.1

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CFI-H82 (45W)
IA: TDC=86A, Icc Max=140A, loadline=1.8mohm
GT: TDC=25A, Icc Max=32A, loadline=2.7mohm
SA: TDC=10A, Icc Max=11.1A, loadline=10.3mohm

CFI-H62 (45W)
IA: TDC=80A, Icc Max=128A

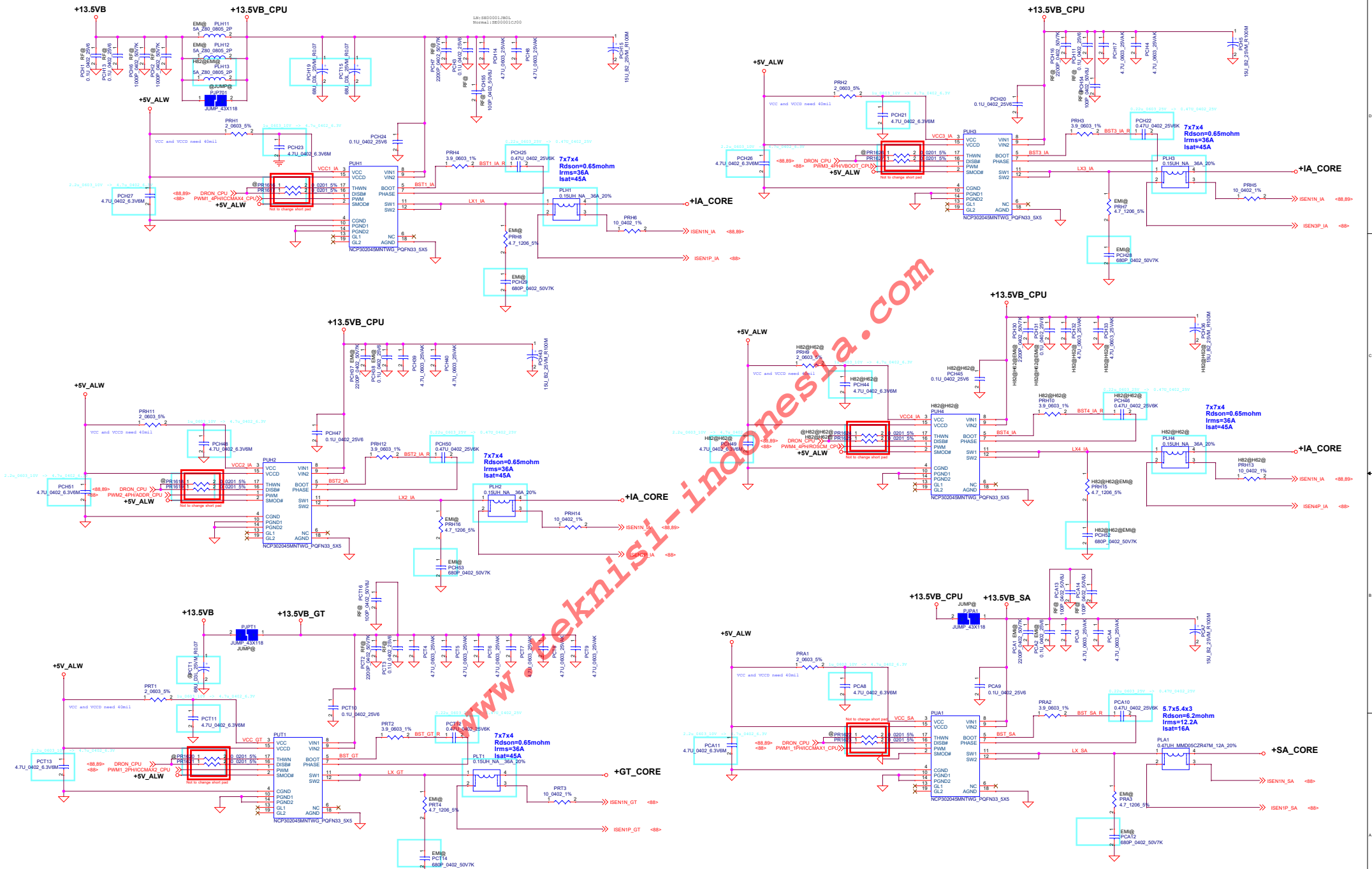
CFI-H42 (45W)
IA: TDC=60A, Icc Max=86A,

OCF
IA: 166A
GT: 42A
SA: 18.6A
OVP
DAC+370mV

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Compal Electronics, Inc.			
CPU CORE			
Rev	0.1	DB-2283P	
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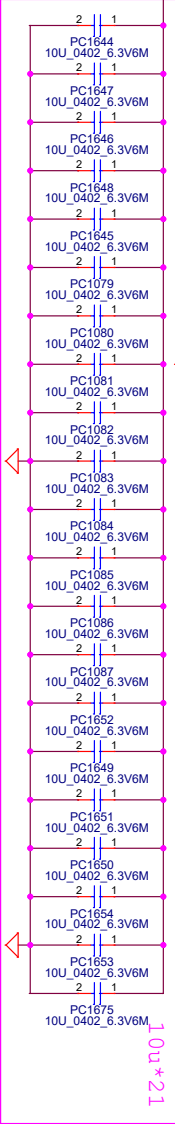
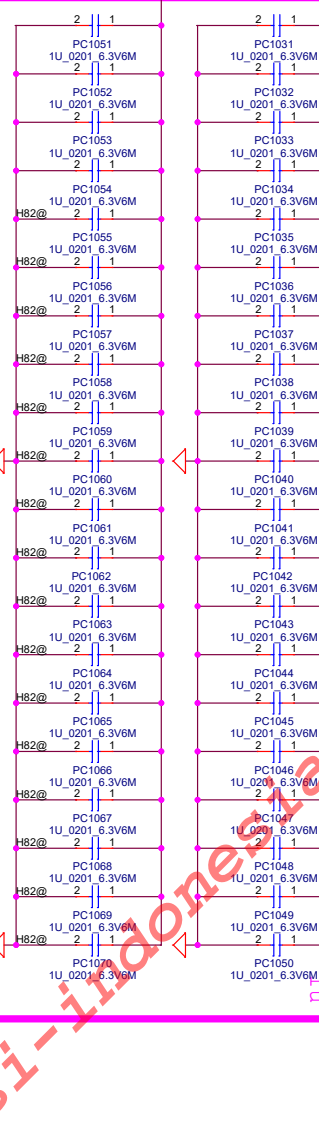
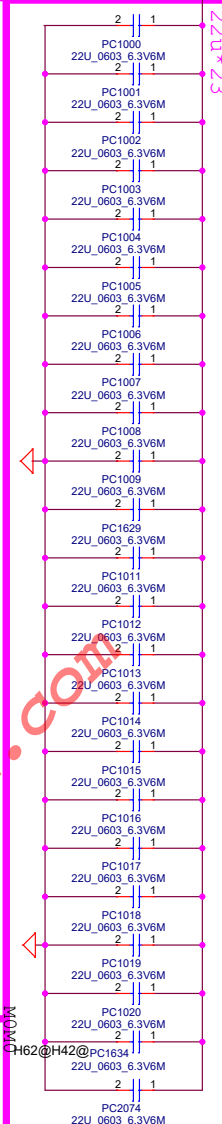
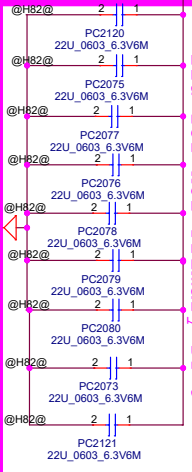
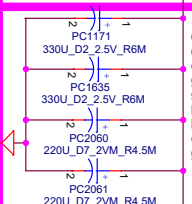
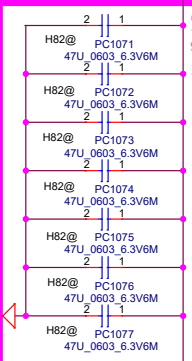
				Compal Electronics, Inc.			
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+IA_CORE

47u*7

330u*220u

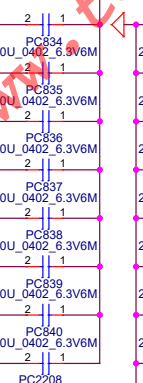
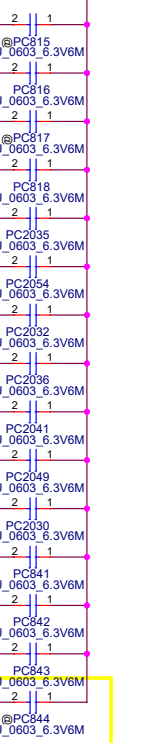
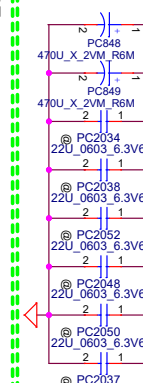
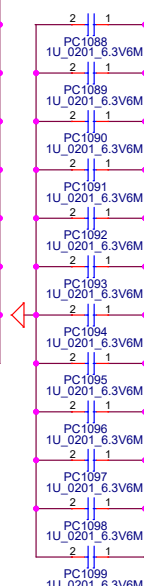
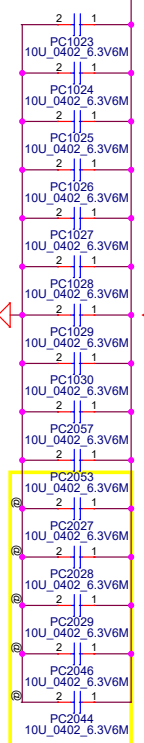
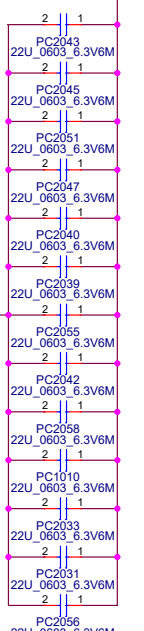
42u for H82 Primary D1*9



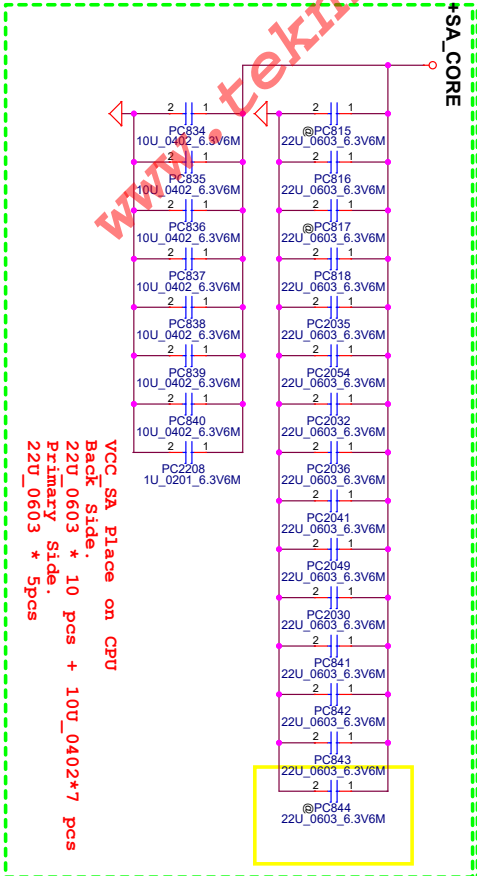
+IA_CORE		H62		H82	
caps(uF)	size	Backside	Primary	Backside	Primary
47	0603			1	7
22	0603	23		22	9(DV)
10	0402	21		21	
1	0201	24		48	
220	D7	2		2	
330	D2		2		2

+GT_CORE

VCC GT Place on CPU
Back Side.
22u 0603 * 6 pcs +10u 0402*10 pcs +1u 0201*12 pcs
Primary Side.
22u 0603 * 7 pcs +470u D2*2 pcs



VCC SA Place on CPU
Back Side.
22u 0603 * 10 pcs + 10u 0402*7 pcs
Primary Side.
22u 0603 * 5pcs



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Reserve

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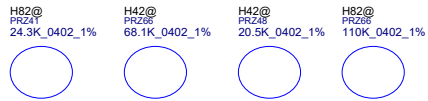
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CPU




OUTPUT CAPS



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Item	Page#	Date	Issue Description	Description			
1	70	2018/05/23	follow BH ARD (v0.5) define	JSD1 connector use Micro SD type,QR1.3 change to gnd			0.1 (X00)
2	44	2018/05/23	PD USB2.0 source from PCH follow X10 NB	PD USB2.0 source change from TBT to PCH depop RT402,403 pop RT400,RT401			0.1 (X00)
3	46	2018/06/05	add TBT type c short protection circuit	implement AR type c short protection circuit ,add RT190~RT197,CT326~CT329,CT95~CT98,RT488~RT491,RT219~RT222			0.1 (X00)
4	43	2018/06/05	change PD and AR power rail	1.PJP6 no solder,RT48 pop 2.add RT399 pop,RT398 depop for +3.3V_VDD_PIC option 3.add RT482 depop,RT483 pop for +3.3V_VDD_PIC_PDA option,remove PJP7			0.1 (X00)
5	38	2018/06/05	follow NB JEDP1,JTS1 pin define	remove LV27,DV4,JIR1,UH1.M6,UH1.N8 add JIRTS1,pin define follow NB add RV733,RV732 JEDP1.1 +5V_TSP- +TS_PWR_SRC JEDP1.2 USB20_N9_R- NC JEDP1.3 USB20_P9_R- NC QV8.1 +5V_TSP- +TS_PWR_SRC check TS_INT#,TS_I2C_SDA,TS_I2C_SCL GPIO			0.1 (X00)
6	11	2018/06/08	power follow compal naming rule,HW synchronize change net name	VSS_IO_SENSE- VSSIO_SENSE VCC_IO_SENSE- VCCIO_SENSE VSS_GT_SENSE- VSS_SENSE_GT VCC_GT_SENSE- VCC_SENSE_GT VCC_SA_SENSE- VCC_SENSE_SA VSS_SA_SENSE- VSS_SENSE_SA VCC_SENSE- VCC_SENSE_IA VSS_SENSE- VSS_SENSE_IA +PWR_SRC +13.5VB +TBTA_Vbus_1- +20V_TBTA_Vbus_1			0.1 (X00)
7	56	2018/06/08	change audio codec solution to ALC 3204	follow ARD implement ALC 3204 schmatic(UA1)			0.1 (X00)
8	66	2018/06/08	follow USH/B pin define	JUSH1 pin define follow NB,support USH/B CV3 remove LZ2,CZ61 add RZ1414 RZ114 pop 1.JUSH.1 +PWR_SRC_R- POWER_SW#_MB_USH 2.JUSH.2 NC- FPR_RST#_USH 3.JUSH.4 POA_WAKE#_R- USB20_N4_USH 4.JUSH.5 EC_FPM_EN- USB20_P4_USH 5.JUSH.17 NC- +5V_ALW 6.JUSH.21 USH_RST#_R- FPR_SCAN_INT#_R 7.JUSH.25_GND- NFC_ACTIVITY_STATUS#_R			0.1 (X00)
9	68	2018/06/08	Reserve for SSD storage protection power gate control schematic	1.add PJP1604,RN131 RZ110 for +3.3V_SSD power option 2.add RN129 for SSD protection 3.add UZ53,UZ54,RZ1471,RZ1472,CZ305,CZ306,RZ1474,QZ24 (depop) 4.check SSD_SCP#,SSD_SCP_PWR_EN GPIO			0.1 (X00)
10	62	2018/06/08	add M-BIST HW Circuit	1.remove HDD_LED_MUX circuit(remove QZ2,RZ25) 2.add M_BIST circuit(DZ12,RZ1415,RZ1482,RZ1413,CZ218,QZ21,QZ3,RZ25)			0.1 (X00)
11	17	2018/06/08	BOM option for VPRO,non-VPRO	1.UC6 change to SA00005VV20(follow NB) 2.NVPRO@ RH352,RH353,UC6,CH270,RH177,RH657,RH658,RH659,RH660,UC5,RH178,RH179,RH181,RH183,RH184 3.VPRO@ UC5,RH178,RH179,RH181,RH183,RH184,UL1 4.add NVPRO_LAN_CHIP_UL1 SA00009340L 5.RZ59,RZ58,RZ60 change to 33 ohm and BOM structure NA			0.1 (X00)

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12	18	2018/06/08	glitch schematic	SIO_SLP_S0# add RH640 100k PU(depopped) to +3.3V_ALW_PCH	0.1 (X00)	
13	62	2018/06/08	follow NB AR use clip type shielding can	SHDCAN footprint change to SION_C7521R 1P-T add 4 clip for AR,PD location:CLP1,CLP2,CLP3,CLP4	0.1 (X00)	
14	16	2018/06/08	change crystal size,follow NB	YH2 SJ10000VK00- SJ10000XF00 YV1 SJ10000EQ00- SJ10000ZL00	0.1 (X00)	
15	51	2018/06/08	RJ45 2 LEDs	remove UL2,QL1 add RL20 UL1.27 LOM_SPD100LED_ORG#- LOM_CONNLED_GRN# UL1.25 change to TP(LOM_LED2) QL1.4 LOM_SPD100LED_ORG#- LOM_CONNLED_GRN# QL1.3 LED_100_ORG#- LED_GRN# JLOM1 follow NB_180615	0.1 (X00)	
16	58	2018/06/19	naming change	UE1.K4 DCIN1_EN- DCIN2_EN UE1.L12 DCIN2_EN- DCIN1_EN UE1.M6 VBUS1_ECOK- VBUS2_ECOK UE1.N3 VBUS2_ECOK- VBUS1_ECOK UE1.L7 1.8V_1.0V_PWRGD- PRIM_PWRGD (add RE361)	0.1 (X00)	
17	63	2018/06/19	add programming circuit	JSPI1.17 add net PROM BIOS_R add RZ401,RZ400 to PCH_RSMRST# RH185 depop	0.1 (X00)	
19	73	2018/06/26	USB3.0 length over spec,add repeater	add UI6 USB3 repeater and related components	0.1 (X00)	
20	17	2018/06/28	Reserve for Panel side TS PH voltage problem schematic	1.add RH566 pop 2.add QH8,RH104 depop 3.JEDP1.5 TOUCH_SCREEN_PD# - TOUCH_SCREEN_PD#_R	0.1 (X00)	
21	63	2018/06/28	X10 KB support KB disabel function	1.add RZ1475 pop 2.JKBTP1.10 add net TP_DISABLE#_R 3.TP_DISABLE# add net to EC	0.1 (X00)	
22	21	2018/06/28	follow CFL H PDG 1P8 page.623	1.+1.0V_XTAL add 2x 22uF 0603 (add CH349 depop) 2.+1.0V_AMPHYPLL add 2x 22uF 0603 (add CH350 depop) 3.CH32 change to 1x4.7uF 0402	0.1 (X00)	
23	21	2018/07/03	follow CFL H PDG 1P8 page.623	1.+1.0V_XTAL Series Inductor 0603 2.2 Uh depop(LH421) 2.+1.0V_AMPHYPLL Series Inductor 0603 2.2 Uh depop(LH423)	0.1 (X00)	
24	12	2018/07/03	+1.0V_VCCSFR add LPP	add LC562depop,RC422 pop	0.1 (X00)	

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25	58	2018/07/12	GPIO modify	remove RE566,RH639,RH638,RH624,RH360,RH330,RH621,RH622,RH623,RE101,RH207,RH322,RH425 add RE340,RH661 1.UE1.D1 HDD_EN_EC → TBT RESET_N_EC 2.UE1.D6 EC_FPM_EN → FREE 3.UE1.E4 POA_WAKE# → FREE(VCI_IN3#) 4.UE1.J6 CG6 ACPI_CHECK → NB_MODE# 5.UE1.K1 PCH_PLTRST#_EC → WWAN_GPIO_CTRL 6.UE1.L8 TBT_RESET_N_EC → FPR_SCAN_INT# 7.UH1.AP21 RTD3_CIO_PWR_EN → FREE 8.UH1.AE43 NC → RTD3_CIO_PWR_EN 9.UH1.AR32 TBT_RTD3_WAKE# → NC 10.UH1.T47 NC → TBT_RTD3_WAKE# 11.UH1.BE20 LPSS_UART2_TXD → FREE 12.UH1.AW21 CNV_EN# → FREE 13.UH1.BE23 PCH_TBT_PERST# → FREE 14.UH1.AM48 FREE → PCH_TBT_PERST#		0.1 (X00)	
26	17,18	2018/07/23	3.3V_CAM_EN# change,TBT_RTD3_WAKE# reserve	1. 3.3V_CAM_EN# contact to PCH GPP_D2(pin BE18) 2. Reserve 0ohm for TBT_RTD3_WAKE# to PCH GPD7(pin BE41) add RC834,RH662@,RH663 change name RH602.1 TBT_RTD3_WAKE#_GPD7 change name RH661.2 TBT_RTD3_WAKE#_K18		0.1 (X00)	
27	58	2018/07/24	remove EC VTR3 3V3 power jump	1.remove PJP21 2.+1.8V_3.3V_ALW_VTR3 → +1.8V_ALW_VTR3		0.1 (X00)	
28	44	2018/07/24	Vendor review,PD cc cap value change	CT85,CT86 470pF → 220pF RT98 0_ohm → 100k_ohm		0.1 (X00)	
29	12	2018/07/25	VCCPLL bead stuff	VCCPLL LC562 stuff,RC422 unstuff		0.1 (X00)	
30	16	2018/07/25	ESD reserve Components	reserve CH554,CE548,CC549,CH550,CH551,CH552,CC556,CH553,DA9,DA10,DZ13,CC557,CC558		0.1 (X00)	
31	17	2018/07/26	follow NB ROM part change	1.UC5 VPRO use SA00009RI10 2.UC5 NVPRO use SA00003X910 3.UC6 NVPRO use SA00005VV20		0.1 (X00)	
32	38	2018/07/31	EMI change choke size	LZ1,LI7,LI3,LI4 → SM070005U00		0.1 (X00)	
33	12	2018/07/31	power name change	1.+VCC_CORE → +IA_CORE 2.+VCC_GT → +GT_CORE 3.+VCC_SA → +SA_CORE		0.1 (X00)	
34	9	2018/08/03	change DDI port	1.(DDI1) HDMI→ AR_P0 2.(DDI2) AR_P0→ AR_P1 3.(DDI3) AR_P1→ AR_P2		0.1 (X00)	
35	44	2018/08/08	Change PD controller to 65982DD	Change UT5 part to SA0000C8000 from SA0000BIJ00.		0.1 (X00)	
36	66	2018/08/08	Change ST TPM to ST33HTPH2032AHC1	Change UZ12 part to SA0000C5G10 from SA00009S040.		0.1 (X00)	
37	16	2018/08/10	follow CFL H PDG 24MHZ topology	remove RH437,direct connect		0.1 (X00)	
38	62	2018/08/14	follow NB M_BIST schematic	1.DZ12,RZ1413 unstuff 2.add RZ1482(M_BIST_R) PU +3.3V_ALW 3.CZ218 change to 2.2uF		0.1 (X00)	
39	17	2018/08/14	not support KBL H	remove RH171		0.1 (X00)	
40	56	2018/08/14	codec bom modify follow NB	RA53 stuff,RA54 unstuff		0.1 (X00)	
41	17	2018/08/14	WWAN_PWR_EN connect to PCH	1.WWAN_PWR_EN need connect to PCH pin GPP_D0 2.WWAN_PWR_EN change net name to WWAN_FULL_PWR_EN		0.1 (X00)	
42	14	2018/08/14	CNVI PDG update	RZ1382,RZ1384 change to 33 ohm,close to PCH		0.1 (X00)	
43	52	2018/08/22	naming change	1.+TS_PWR_SRC → +TS_PWR 2.remove RE361,PRIM_PWRGD → 1.8V_1.0V_PWRGD 3.RZ1483 change to unstuff		0.1 (X00)	
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44	44	2018/08/22	follow compal naming rule	TBTA_TOP_P → SW_TBT_A_USB20_P2 TBTA_TOP_N → SW_TBT_A_USB20_N2 TBTA_BOT_P → SW_TBT_A_USB20_P1 TBTA_BOT_N → SW_TBT_A_USB20_N1 TBTA_TOP_P_R → SW_TBT_A_USB20_P2_R TBTA_TOP_N_R → SW_TBT_A_USB20_N2_R TBTA_BOT_P_R → SW_TBT_A_USB20_P1_R TBTA_BOT_N_R → SW_TBT_A_USB20_N1_R	0.1 (X00)	
45	52	2018/08/28	implement support 7360 card schematic	1.add component RZ1397,QZ19,RZ1398,RZ1399,UZ51,CZ216,RZ1395,RZ1396,RZ1394,RZ1403,RZ1404,CZ217,RZ1406, RZ1401,RZ1481,RZ1480,RZ1402,RZ1405,RZ1400,RZ1393,RZ1450,RE340,RC840,RC756,UZ52 2.JNGFF2.54 PCIE_WAKE# → WWAN_PEWAKE# 3.JNGFF2.67 NC → WWAN_BB_RST# 4.UE1.K1 NC → WWAN_GPIO_CTRL add GPIO UH1.BC17 → WWAN_GPIO_PERST# UH1.BF35 → WWAN_BB_RST# UH1.BD17 → WWAN_GPIO_WAKE#	0.1 (X00)	
46	58	2018/08/30	align NB modify schematic	1.reserve RE821 SSD_SCP# PU to +3.3V_ALW 2.WWAN reserve RZ1484,RZ375 PU 3.reserve CN77 22U for support Teton Glacier in the future	0.1 (X00)	
47	54	2018/08/30	HW internal review	1.UT11.22 UT12.22 PWD pin add test point for test 2.UZ5 remove?need HW meeting discuss 3.VCCST_PWRGD not need connect to EC,remove RE308,RE552,UE1.K10 change name to SLP_WLAN#_GATE 4.NFC_ACTIVITY_STATUS# not need connect EC to USH connect,UE1.E4 change name to VCI_IN3# 5.RE401 stuff for RTC_DET# PU to +1.8V_ALW_VTR3 6.not use LPC,remove PCH_PLTRST#_EC net,remove RH244,RE375 7.remove RE560,ESPI_RESET# direct connect to JESPI 8.remove DZ7,RZ87,USH_DET# direct connect to JUSH1 9.remove NVME_LED#,SATALED#,RN100,RH380,RN101 10.for reduce power consumption,stuff RN227 11.UZ23,CZ129,CZ130 unstuff for reserve 12.JUSB2,JUSB3 VBUS add 150uF CI103,CI104 13.change name TP_DISABLE# → PTP_DISABLE#,TP_DISABLE#_R → PTP_DISABLE#R 14.for S3 no power issue not use,remove QZ4,RZ370 15.align NB,RZ1484 stuff,RZ379 unstuff,RZ375 remove 16.remove RV1652,CV1639,name change DGPU_PWR_EN_RC → DGPU_PWR_EN_D 17.remove QV24,RV667	0.1 (X00)	
48	52	2018/09/03	WWAN_GPIO_PERST# PU power change	RZ1405 PU change to +3.3V_ALW add RZ1485 PU change to +3.3V_RUN unstuff	0.1 (X00)	
49	52	2018/09/04	GPIO name change	1.HDD_EN_PCH → PCH_HDD_EN	0.1 (X00)	
50	68	2018/09/04	support optane SSD add cap	1.CN60 68P_0402 change to 0.01u_0402 2.add CN80,CN81,CN84,CN82 0.01u_0402 3.add CN86 0.1u_0402	0.1 (X00)	
51	18	2018/09/04	PDG eSPI series resistance update	RC366,RC367,RC368,RC369 change to 0 ohm RH97 change to 33 ohm	0.1 (X00)	
52	56	2018/09/04	Space limitation,remove audio load SW	remove UZ5,PJP15,PJP16,CZ125,CZ126,CZ127,CZ128 RH345 change to @	0.1 (X00)	
53	15	2018/09/05	save layout space	delete:T37,T38,RH60,RH375,RE547,RL70 downsize to 0201:RH65,RH187,CC32,RH133,RH132,RH10,RH11,RH13,RH14,RH15,RH16,RH17,RH309, RH316,RH378,RH348,RH350,RH441,RH203,RH204,RH424,RH309 change to test point:RH99(T424)	0.1 (X00)	
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68	62	2019/01/03	DFX request	15" add Fiducial Mark FD8	0.3 (X02)
69	52	2019/01/03	RF BOM option	1.LI9 depop 2.RI49,RI50 change to use SM01000TP00 3.RI49,RI50 change name to LI49,LI50	0.3 (X02)
70	58	2019/01/03	reserve the CNVi detect on GPP_D20	1.remove test point T269 2.reserve 0 ohm RE828 3.RE828.1 CNVI_EN# connect to PCH GPP_D20 4.RE828.2 connect to CNV_DET#_EC 5.CNVI_EN# reserve 75K PD(RH868)	0.3 (X02)
71	52	2019/01/03	INTEL suggest REFCLK_CNV need impedance control	1.remove 0 ohm RZ371,RZ81 2.remove net ISH_UART0_RXD,ISH_UART0_TXD,ISH_UART0_CTS#,ISH_UART0_RTS#	0.3 (X02)
72	56	2019/01/03	DFX request	DA4,DA5 change footprint to 1N4148WS-7-F_SOD323-2	0.3 (X02)
73	59	2019/01/03	board ID change to X02	board ID RE79 change to X02 62K ohm	0.3 (X02)
74	38	2019/01/03	align NB reserve fuse	1.reserve FZ4,FZ5,RZ1486 2.add RZ1487,RZ1488 0 ohm	0.3 (X02)
75	23,24	2019/01/03	DFX request	JDIMM1,JDIMM2 change footprint to FOX_ASAA821-H4RB5-7H_260P	0.3 (X02)
76	38	2019/01/03	to avoid camera & DMIC lost after ESD test	pop DA9,DA10	0.3 (X02)
77		2019/01/03	0 ohm change to short pad	location reference X10 BH DVT2.0 0 Ohm_190104.xlsx	0.3 (X02)
78	66	2019/01/03	align LKE reserve TPM power source	+3.3V_VPS_UZ12 reserve 0 ohm RZ1489 to +3.3V_ALW	0.3 (X02)
79	38,58	2019/01/03	ESD request	reserve cap 0.1u TOUCH_SCREEN_PD#_R (CV113) CAM_MIC_CBL_DET# (CV112) BIA_PWM (CV111) EDP_HP (CV110) TOUCH_SCREEN_DET# (CV109) IR_CAM_DET# (CZ1203) CE548 from 0.1u 0201 change to 4700p 0402	0.3 (X02)
80	7,38	2019/01/03	ESD request	CC306,CC308,CC302,CH551,CC305,CC304,CC303,CV113,CV112,CV110,CV109,CZ1203 from reserve to add 0.1uF cap CE548 from 47nF reserve to add 47nF	0.3 (X02)
81	7,18	2019/01/03	ESD request	RC124 depop,CC307 100pf pop CH266 100 pf POP	0.3 (X02)
82	52	2019/01/03	BOM option for non WWAN SKU	HU non WWAN SKU BOM option 1.LI8,LI16,LI17,CZ198,CZ42,CZ41,CZ23~CZ26 change to WWANRF@ 2.UZ29,CZ154,CZ155,RZ360,CZ150,CZ151,CZ152,CZ153,CZ10,CZ11,RZ43,DZ5,DZ6,CZ37,RZ1406,CZ217,UZ52,RZ1405,RZ1400,UZ51,CZ216,QZ19,RZ1399,RZ1397,QZ8,CZ17~CZ21 change to WWAN@	0.3 (X02)

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